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Aging-Induced Failure Prognosis via Digital Sensors

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ABSTRACT

Aggressive scaling continues to push technology into smaller feature sizes and results in more complex systems in a single chip. With such scaling, various robustness concerns have come into account among which the change of circuits' specification during their lifetime, so-called device aging, has received a lot of attention. Due to aging, the electrical behavior of transistors deviates from its original intended one resulting in degrading the chip's performance, and ultimately the chip fails to provide correct outputs. Accordingly, prognosis of circuit performance degradation during the runtime, before the chip actually fails is highly crucial in increasing the reliability of chips. Accordingly in this paper, we develop a machine-learning based framework that, leveraging the outcome of embedded time-to-digital-convertors (so-called digital sensors), predicts aging-induced degradation. This information can be used to prevent chip failures via deploying Dynamic Voltage and Frequency Scaling (DVFS).

1 INTRODUCTION

Faster operations and low power usage have been made possible via moving toward smaller feature nodes. However, along with such advantages, the degradation of the integrated circuits' performance over time has received the lion's share of attention. Such degradation, the so-called device aging, can jeopardize both the reliability and security of the integrated circuits [2, 14]. Indeed, device aging mainly increases the paths' delay and ultimately results in violating the timing guard-band and corrupting device output. Thereby, it is highly important to prognose the aging-induced failures before the circuit's output is affected.

In practice, devices are designed to work under well-defined conditions; in particular, within PVT (acronym short for "Process, Voltage, and Temperature") corners. During their lifetime, devices go through dynamic environmental conditions, i.e., they experience different voltages and temperatures. As the rate of Integrated circuits (ICs) performance degradation is impacted by a variety of the IC operating conditions, such as voltage bias, temperature, and workload distribution, aging prognosis is not straightforward and needs to take into account the history of these factors [12, 13].

The classic aging prognosis schemes mainly utilize lookup tables to record the history of operating conditions and use this data to predict aging degradation rate via machine learning models [8, 19]. However, as the operating conditions can change frequently during the runtime, using such method is challenging. Ring-oscillator based sensors have been also proposed in literature for aging prognosis [3]. However, these sensors suffer from aging-induced delay change, resulting in metastability and corrupting the sensor output [13].

In [18], electromagnetic signatures have been used to predict aging effects in ICs. However, this approach requires costly external equipments. Agrawal et al. [3] proposed predicting circuit's failure using aging sensors that capture the impact of IC aging based on the observation of guardband timing violations. In [11], a dynamic voltage scaling (DVS) approach, nicknamed "Razor", has been proposed which monitors the delay-based error rates during circuit operation and uses such data to adjust the supply voltage.

Machine Learning (ML) based aging prediction algorithms have also recently received a lot of attention as they can efficiently predict aging-induced failures with generalization capability [2, 15]. The authors of [12] proposed an ML-based approach to predict aging degradation during runtime based on equivalent aging time. Huang et al. [13] proposed an ML-based approach that uses the historical operating condition parameters from on-chip sensors to detect aging-induced failures. The authors in [2, 15] deploy machine learning for aging prognosis. In these methods, a model is trained using a set of operating condition parameter values (e.g., workload and temperature) and aging indicator values (e.g., the delays of critical paths). The trained model is then used to predict the aging indicator values for any given operating condition. However, these models fail to consider that operating conditions (e.g., temperature) change over time. This can result in an inaccurate aging failure prediction and even unexpected failure (e.g., circuits may fail earlier with higher-than-expected temperature) [12]. Please note that the rate of aging degradation is not linear over time. The impact is high initially (for the first few months of operation) and then saturates over time. This makes the aging prognosis and prediction of the device failure time more challenging.

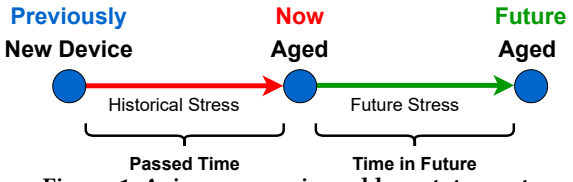


Figure 1: Aging prognosis problem statement.

To fill the gap, in this paper we not only opt to quantify the aging rate in the current time but also aim at predicting the aging rate in the future given that the circuit continues working under the same voltage and temperature from now on. To clarify, we take into account that the temperature and voltage values may have changed multiple times during the circuit operation in the past, and consider the effect of those changes in quantifying the aging rate at each point in time. Meanwhile, we move one step further and

quantify the aging rate in the future given that the circuit continues operating at the same voltage and temperature from the time we quantify the aging rate. Figure 1 shows the high-level view of this discussion. The device degradation in the current time depends on its historical environmental stress, yet future degradation depends on the degradation that the device faced in history and the environmental condition it will face during its lifetime in future. This assumption infers that similar future environmental condition may have different aging degradation rates due to previous historical environmental variations.

In sum, in this research, we propose a ML-based scheme that performs aging prognosis based on the data extracted from the time-to-digital converters (so-called digital sensors hereafter) residing in the circuit for this purpose. This information will assist efficient DVFS management schemes to reduce circuit aging-induced failures. Indeed, removing the need for storing the history of operating conditions in memory for aging prognosis makes our approach lightweight and more appealing. The contributions of this research include:

- Removing the need for recording the history of operating conditions to be used for aging prognosis;
- A low-cost approach that considers the impact of voltage and temperature in device aging altogether not as individual entities;
- A novel aging prognosis methodology using on-chip digital sensors and machine-learning schemes;
- Extensive experimental results representing how the sensor outcome changes in different operating conditions and how it can be used for aging prognosis.

2 PRELIMINARY BACKGROUNDS

2.1 Device Aging

Device aging results in performance degradation and eventual failure of digital circuits over time [7, 17]. Among the aging mechanisms, Bias Temperature-Instability (BTI) (including both NBTI and PBTI referred to negative and positive BTI, respectively) and Hot Carrier Injection (HCI) are two leading factors in performance degradation of digital circuits [20]. Both mechanisms result in increasing switching and path delays in the circuit under stress; leading to timing violations and finally wearing out of the system.

BTI Aging: NBTI and PBTI affect PMOS and NMOS transistors, respectively. In practice, a PMOS transistor experiences two phases of NBTI depending on its operating condition. The first phase, so-called stress phase, occurs when the transistor is on ($V_{gs} < V_t$). In this case, the positive traps generated at the Si-SiO_2 interface lead to the threshold voltage increase of the transistor. The second phase, the so-called recovery phase, occurs when the transistor is off ($V_{gs} > V_t$). Here the threshold voltage drift that occurred during the stress phase is partially recovered. Figure 2 shows the threshold voltage change of a transistor that is always under the stress versus the transistor that is under stress and recovery every other month. PBTI affects NMOS transistors in a similar way that NBTI affects PMOS transistors. The physical parameters of the transistor, supply voltage, temperature, and stress time all contribute to the amount of aging-induced voltage drift caused by NBTI and PBTI [4, 16].

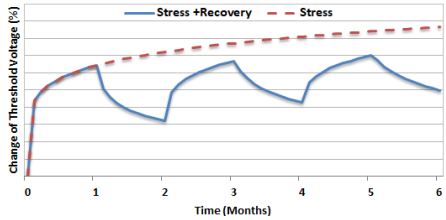


Figure 2: Threshold-voltage shift of a PMOS transistor under NBTI effect [10].[1]

HCI Aging: NMOS transistors are affected by HCI mechanism when hot carriers get injected into the gate dielectric during transistor switching and remain there. HCI depends on switching activity and deteriorates the circuit performance by shifting the threshold voltage and the drain current of transistors under stress [17].

2.2 Digital Sensors

A digital sensor can be realized via inserting artificial critical paths (as simple as delay chains) into the chip logic such that if the chip is operated in abnormal conditions, setup time violations occur in the first place on the sensor's intentionally long path [5]. Figure 3 exhibits the sensor deployed in this paper which consists of n_0 leading inverters followed by n_1 inverters each feeds a D flip-flop to characterize the sensor outcome. The first inverter is fed by a Toggle flip-flop and all flip-flops operate under the same clock which is the clock signal under which the main circuit also operates. The digital sensor design methodology, i.e., determining the number of flip-flops and inverters, has been discussed in detail in [5]. However, we replaced buffers of [5] with inverters in this paper to increase the resolution of our characterization. Moreover, as depicted in Fig. 3, the flip-flop outputs are collected from the Q and $\overline{Q}$ pins in every other flip-flop. This helps to characterize the digital sensors that have been constructed using inverter similar to the digital sensors realized via buffers. Note that this sensor is resided in the chip along with the main circuit to monitor the circuit behavior; in our case it is used for aging prognosis as will be discussed in the following sections.

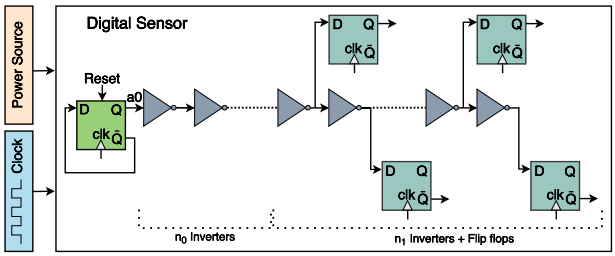


Figure 3: Targeted digital sensor architecture.

Digital Sensor Characterization: To characterize our sensor and in turn to monitor the operating conditions, we deploy a metric, so-called Average Flip-flop Number (AFN), that is extracted based on the flip-flop outputs in each voltage and temperature combination at each clock frequency. As the propagation delay of the inverters included in the delay chain of our sensor (shown in Fig. 3) is changed

[1]Values on Y axis are not shown to make the graph generic across different silicon foundries and technological nodes.

in different voltage, temperature, and clock frequency, the AFN metric can be a good representative for each operating condition.

In each clock cycle CC_i, when $a0$ signal is fed to the sensor, the first $FN_i - 1$ flip-flops' outputs would be in phase A (say for example $0 \rightarrow 1 \rightarrow 0$) and the remaining flip-flops' outputs would be in the complementary phase $\overline{A}$ (say $1 \rightarrow 0 \rightarrow 1$), where FN_i corresponds to the flip-flop index at which step $\overline{A}$ begins in the clock cycle CC_i. Recall that we extract the values of Q and $\overline{Q}$ in every other flip-flip resided in the chain alternatively. This nullifies the impact of inverters. Note that in different (V,T) configurations this FN_i index changes. For characterization, FN_i values are collected in few consecutive clock cycles and average is evaluated. This average value is called AFN and used for characterization. Figure 4 exhibits the outputs of the flip-flops resided in the sensor shown in Fig. 3 in specific temperature and voltage for n_0=4 leading inverters following by n_1=112 inverters and flip-flops. Here, AFN=83 as the first flip-flop that does not experience a phase change compared to its previous ones is the 83rd flip-flop.

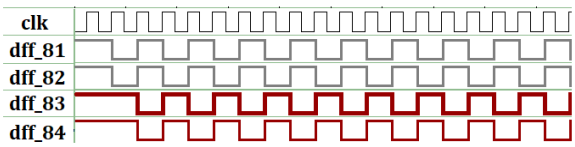


Figure 4: Waveforms of Fig. 3 in V=1.2V and T=30°C.

Figure 5 depicts how different operating conditions affect AFN. For slower conditions, i.e., high temperatures and low voltages, AFN is lower. On the other hand, AFN is higher in high voltages and low temperatures where circuit operates faster. As AFN value is related to both voltage and temperature as a pair, same AFN value may represent different operating conditions [6].

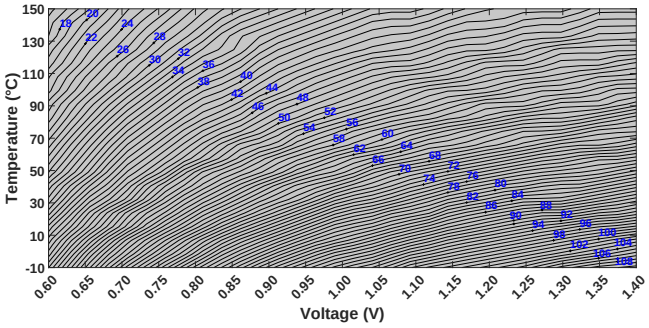


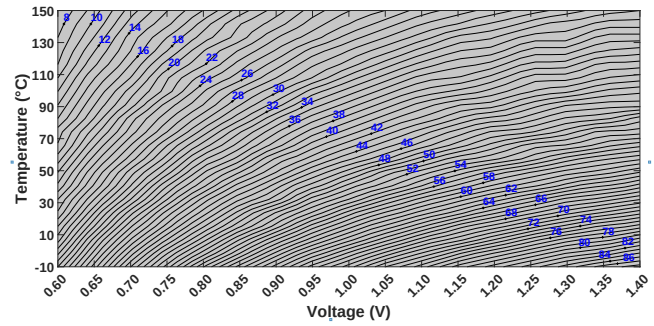
Figure 5: AFN values extracted from the new sensor in different environmental conditions.

3 AGING IMPACTS ON THE SENSOR OUTCOME

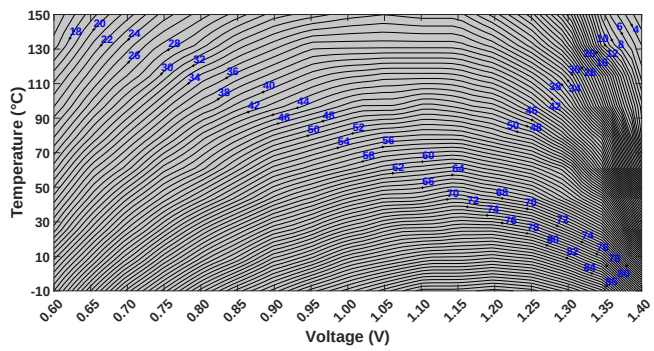
3.1 Aging-Induced AFN Changes

The sensor becomes slower over time due to the aging-induced changes. Accordingly, the AFN characteristic of the sensor decreases over time in different rate when working under the different operating conditions. To clarify how AFN changes over time, we show two examples in Fig. 6(a) and Fig. 6(b). The former shows the AFN values in different (V,T) conditions during the measurement for the sensor of Fig. 3 after 7 years of usage given that the circuit was operating under V=1.2V and T= 100°C for the whole 7 years. As shown, AFN decreased compared to its nominal condition (when it was new; recall Fig. 5). For example: For new device, at Vdd 1.0V and Temperature 85°C, AFN was 53 (Fig. 5). However, it decreased to 38 after 7 years of aging.

Our second example, shown in Fig. 6(b), represents the AFN value after 7 years of aging in different (V,T) conditions during the measurement given that the circuit was operating in the very same (V,T) conditions during the 7 years of usage. In this case, as shown, AFN decreased less in areas where voltage and temperature are low, on the other side AFN decreased more in cases of high voltage or high temperature.



(a) AFN at 7 years, stress: Vdd=1.2V and Temp.= 100°C.



(b) AFN at 7 years, stressed with same voltage and temperature as measurement.

Figure 6: Change of AFN under different stress conditions during aging.

The takeaway point from this observation is that the AFN value changes depending on the stress the sensor experienced. Thereby, we can utilize AFN degradation as a representation of aging-induced device degradation. This relaxes the requirement of storing the circuit operating condition history for aging prognosis.

3.2 Effect of Dynamic Environmental Variation on Aging-Induced AFN Change

The amount of aging-induced degradation a circuit experiences depends on environmental conditions such as operating voltage and temperature, as well as its workload during the course of usage. However, these parameters are not fixed during the lifetime, i.e., the device can experience dynamic environmental conditions and workloads. Indeed, most of the existing aging prognosis methods countermeasures fail to consider dynamic operational conditions.

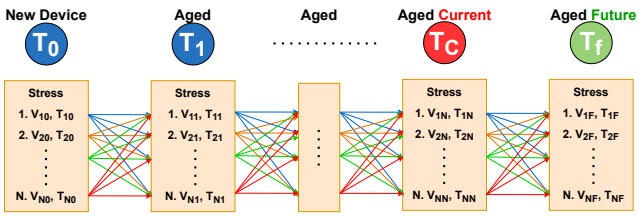


Figure 7: Dynamic change in environmental conditions.

Figure 7 represents the dynamic environmental conditions a device can go through during different points in time. Time T_0 refers to time=0 when the device is new. The figure simply shows that in time 0 (shown as T_0) as well as any subsequent timing duration the circuit may experience a different (V,T) combination. Such history affects the aging rate. However, storing the history of operating conditions is not cost-effective. Fortunately, our digital sensor can sense these dynamic operations accumulatively during the circuit's lifetime.

Figure 8 shows the status of the sensor in three different scenarios of aging condition (each is shown in one row). In all cases, the new sensor was operating at V=1.2V and T=25°C resulting in AFN=84.5. For example: In *Condition A*, the sensor is under more stress considering its high voltage and temperature, thus it experiences higher degradation compared to the other 2 cases where the circuit was under less stress. In practice, it is not possible to determine the stress the circuit experienced, yet we can extract the acculturative impact using the AFN value.

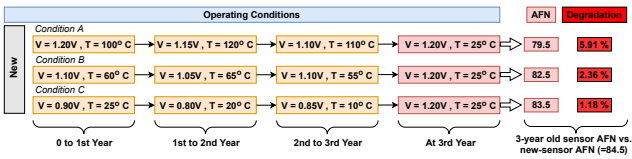


Figure 8: Change of AFN due to dynamic environmental conditions during stress period.

4 PROPOSED AGING PROGNOSIS METHODOLOGY

As mentioned earlier, in this paper we are to perform aging prognosis. In particular, we opt to predict the AFN that the sensor will represent in time T_f (future time) given that we know the AFN in time T_c (current time). However, as shown in Fig. 4 and Fig. 6, the AFN value changes in different voltages and temperatures. In addition, we do not have access to the history of operating conditions. Moreover, aging degradation rate is not constant over time, i.e., the rate is higher in the first few months of device usage. Considering all of these circumstances, we use a differential method to predict AFN value in time T_f assuming that the device operates in the same voltage and temperature between time $[T_c, T_f]$.

Our differential scheme relies on embedding three digital sensors in the circuit to sense the aging-induced changes and in turn to perform aging prognosis. To do so, we deploy a digital sensor and its two replicas where the main sensor is always ON (so-called Always-on Sensor or A-Sensor hereafter) while the replicated sensors, i.e., R-Sensor and RD-Sensor, turn on rarely, thus are affected much less by aging. Figure 9 shows the proposed structure. Note that in our method, all three sensors are resided close to one another, so they sense the same temperature. However, the A-sensor and R-Sensor are fed with Vdd while the RD-Sensor operates under a different voltage: $Vdd - \Delta Vdd$. We considered ΔVdd = 0.2V.

The idea behind having R-Sensor along with A-Sensor is being able to extract the impact of aging during the runtime based on the difference between the AFN values of these 2 sensors. This relaxes the need to store the operating conditions during the time. The RD-Sensor associated with the R-Sensor allows to know the (V,T) conditions as explained in [6]. Consequently, having the pair (R-Sensor, RD-Sensor) as input of the proposed ML-based scheme implicitly considers the impact of (V,T) in the current AFN, i.e., AFN at the time of T_c.

Note that the R-Sensor and RD-Sensor may get ON in a periodic manner or ad hoc (yet rarely). Also, there is a possibility that all three sensors are OFF simultaneously for some time, e.g., when the system in which the sensors are embedded is unplugged from power supply. This does not affect the efficiency of the proposed methodology.

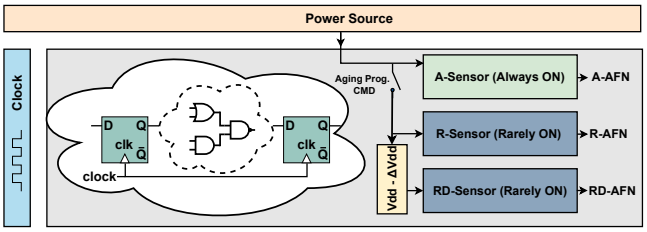


Figure 9: Our proposed sensor setup for aging prognosis.

We then use the AFN values from A-Sensor, R-Sensor, and RD-Sensor (denoted as A-AFN, R-AFN, and RD-AFN) in time T_c to predict the AFN in time T_f>T_c given that the circuit operates in the same (V,T) condition in time $\in [T_c, T_f]$. To do so, we use an ML-model relying on a Neural Network (NN). To train the model, we only need the HSpice simulation data of K triple sensors considering different voltage, temperature, and stress time. This approach has two advantages. Firstly, training the model using multiple sensor pairs' data results in mitigating the effect of process variations in the sensor's outcome as the model learns the process variation effects gradually during the training with multiple triple sensors' data, and benefits from such learning in inferring the A-AFN value in future time T_f. Secondly, conducting Monte Carlo (MC) simulations relieves us from the need for multiple fabricated-chips data.

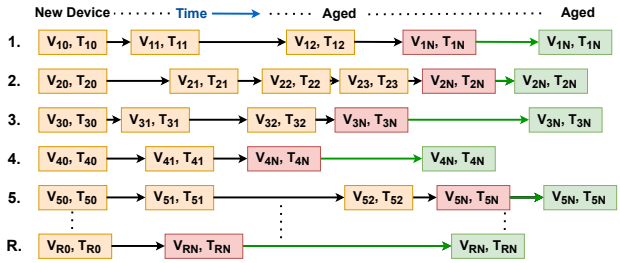


Figure 10: Different sample operating scenarios where red boxes relate to condition at current time T_c, yellow boxes relate to the previous time, and the green boxes relate to the time in future T_f for which aging prognosis is performed.

As mentioned, to build the training data, we use Spice-level simulation for new as well as aged devices. As discussed before, we need to consider scenarios where the circuit goes under different stress phases (referring to the dynamic change of (V,T) during the course of usage).

Figure 10 depicts some sample scenarios where in each case the red rectangle relates to the (V,T) in the current time of T_c, the yellow rectangles relates to the operating conditions the circuit experienced previously (i.e., the (V,T) history). Note that the circuit may experience each (V,T) for different time duration. Finally, the green rectangle relates to the future point of time T_f. Note that as mentioned earlier, we assume that the current and future operating conditions are similar. In other words, we assume that the circuit continues operating in the same condition from the current time.

To build the data needed for the training and testing of the proposed ML-Based aging prognosis schemes, we generate multiple random scenarios and simulate them using HSpice. More details on generating the train and test data is given in Section 5.

In our NN model, the input features include the AFN values of the three sensors at current time (T_c) along with the time difference from the current time (i.e., $T_d = T_f - T_c$) and the label is the A-AFN in time T_f. For example, if we want to know the value of AFN in 4 months from now, we put T_d=4 months. Here, A-AFN is expected to be smaller than R-AFN, as the A-Sensor is always ON so it is aged more than R-Sensor which is rarely ON. Note that the circuit becomes slower when aged; thus, exhibits lower AFN. However, in some cases R-AFN may be higher than A-AFN (specially when the device is new or was used only for a short time) due to the process mismatch between these two sensors.

By predicting the A-AFN that the A-Sensor will generate at time T_f, the user can understand if the circuit is going to be failed at T_f or not. This is done by comparing the extracted A-AFN with the threshold value below which the circuit does not work properly [5]. If the predicted A-AFN is smaller than $AFN_{Threshold}$, then obviously the circuit is going to be failed at time T_f; thus graceful degradation is performed automatically via DVFS mechanism to prevent such failure before it really fails at time T_f. Note that the $AFN_{Threshold}$ is decided based on the worst-case condition that the circuit should work on. More information on deciding about finding such threshold value can be found in [5].

5 EXPERIMENTAL SETUP AND RESULT

Our sensor consists of n_0 = 4 leading inverters followed by n_1 = 112 inverters and flip-flops. The numbers of n_0 and n_1 were decided using Algorithm 2 in [9], however, buffers are changed to inverter for better resolution. We implemented this configuration at the transistor level using 45 nm NANGATE technology [1]. Simulations were conducted using Synopsys HSpice and the built-in HSpice MOSRA Level 3 model was used for assessing the impact of BTI and HCI aging.

We simulated 5814 different cases where each of them included between 1 to 5 stages of stress (selected randomly) each in a randomly selected voltage, temperature, and aging duration. The aging duration was 7 years maximum with the step of 2 months. The circuit continues its operation under the (V,T) it experienced in its last stage of aging up to 7 years of total usage. The voltage Vdd was considered in the range of [0.8V, 1.2V] with the steps of 0.05V, and the temperatures were considered between [-10°C, 150°C] with 5°C steps. We realized different sensor configurations using Monte Carlo simulations to mitigate the impact of process variation on the model's accuracy. We considered Monte Carlo simulations for 4 chips using a Gaussian distribution: transistor gate length L: 3σ = 10%; threshold voltage V_{TH}: 3σ = 30%, and gate-oxide thickness t_{OX}: 3σ = 3%. We generated ≈3,000,000 data points out of the 5814 simulations we conducted using HSpice MOSRA. This is realized by considering different values of T_c and T_d for each of the 5814 scenarios we randomly generated in this study (discussed earlier) where 80% of this data was used for training and the rest for testing.

We used a Neural Network (NN) to predict the future AFN. Its input features include R-AFN, RD-AFN, A-AFN, and T_d (the time difference from the current time we predict the A-AFN for). The Label would be A-AFN at time T_f=T_c+T_d. Our NN model includes 3 hidden layers and one output node. Each hidden layer includes 128 nodes. Activation function is Rectified Linear Unit (ReLU), loss function is Mean Squared Error (MSE), and the Optimizer is Root Mean Squared Propagation (RMSProp). We considered 50 Epocs with validation split equal to 0.2.

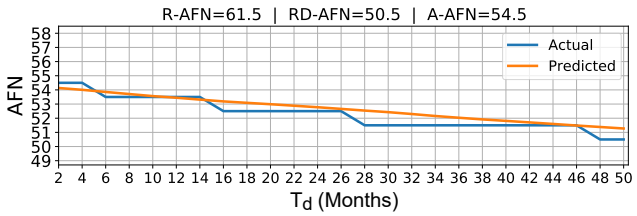
5.1 Experimental Results

Figure 11 represents different test cases where A-AFN is predicted for different values of T_d. On top of each figure, the values of A-AFN, R-AFN, and RD-AFN for the time T_c have been shown. Using these values our NN model predicts the A-AFN at different times in future. As expected, R-AFN has the highest AFN among the three reported in each case. This is because R-Sensor is rarely ON so less aged. Although RD-Sensor is also rarely ON but as it is fed with a lower voltage (i.e., Vdd-0.2V) compared to R-Sensor it has a lower AFN. In Fig. 11 the actual and predicted A-AFN in each point of time are shown in blue and orange, respectively. As depicted, the predicted results are very close to the actual AFN values in all cases. In most cases, the prediction error is in the range of ±0.5 AFN.

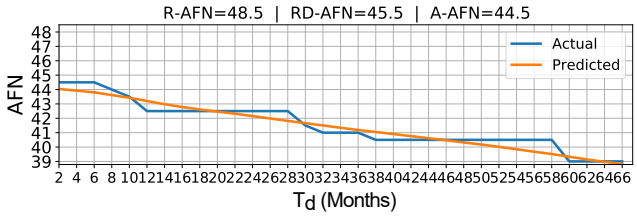
Moreover, we can observe from the test cases that the rate of degradation in the future months is not the same always. As explained in Section 3.2, this is due to the dynamic nature of the environmental condition change. For example, in test case 1 and 2 both degradation rate is high but for test case 3 such rate is low. In practice, in test case 4 there is no visible degradation. This is for the case that the circuit has been already aged for a long time (i.e., tc is higher compared to other cases) and that's why the aging rate is not dominant. These results infer that although predicting aging rate is not straightforward, our proposed method can predict the aging induced delay change through AFN with high accuracy. Indeed, in our NN, the Mean Absolute Error (MAE) during training and validation both were ≈0.40.

Figure 12(a) shows the real A-AFN versus the predicted one. As depicted almost all points reside on the diagonal curve of the figure. Meaning that almost all predicted values match the real AFN values. These results confirm the accuracy of our prediction scheme.

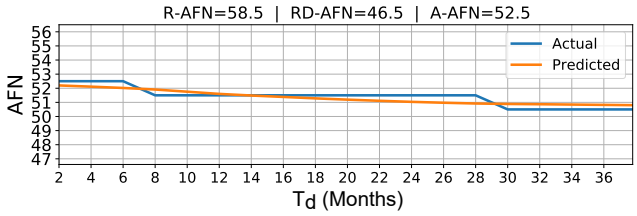
The next set of results, shown in Fig. 12(b), demonstrates the error in predicting A-AFN. As depicted, in most of the cases, the AFN prediction error stays at 0. Also as demonstrated in this figure, the non-zero prediction errors are less than ±2 in most cases. Indeed, on



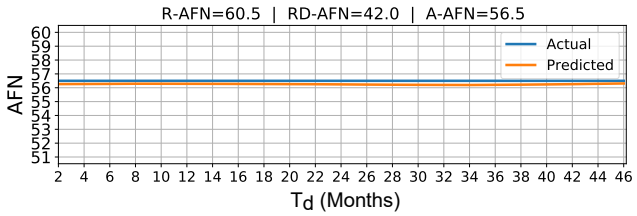
(a) Test Case 1



(b) Test Case 2

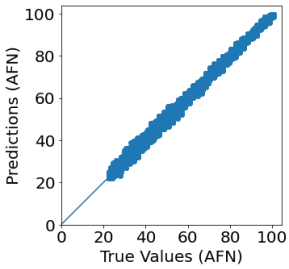


(c) Test Case 3

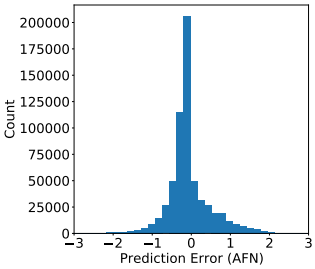


(d) Test Case 4

Figure 11: A-AFN prognosis in 4 different test cases.



(a) True vs. predicted AFN value



(b) Predict AFN Error

Figure 12: Results from prediction model.

average, the absolute error in predicting A-AFN value is ≈ 0.40 AFN. These results again confirm the efficacy of our proposed scheme in aging prognosis through AFN.

The takeaway point from the above observations is that aging-induced degradations can be predicted before it really occurs using our proposed scheme. This information can be used for the graceful degradation of the circuit using DVFS scheme.

6 CONCLUSION & FUTURE DIRECTION

Due to device aging the performance of electronic devices decreases over time, and ultimately the chip fails to provide correct output. Accordingly aging prognosis and graceful degradation of the circuits before they fail are highly important. However, as the aging rate depends on operational conditions, aging prognosis is not straight forward without recording the operating conditions during the runtime. In this paper, we relax such requirements, and via deploying time-to-digital converters predict the aging-induced failures for future time. Our method uses a Neural Network model to perform such prediction. This prognosis can be followed by graceful degradation of the circuit via DVFS mechanism before the circuit really fails.

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