

Challenges in Digital Pre-distortion for 5G pico cells

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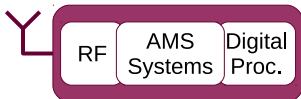
Physical
chips

Circuits
Architectures

Systems

Data Converters Radio Architectures

Interface



Networks and Comm.
Systems



C2S Team – Télécom ParisTech

Physical
chips

Circuits
Architectures

Digital
Processing

Algorithms

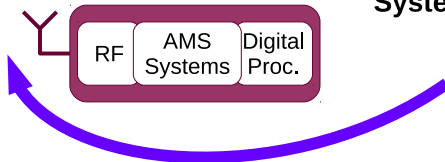
Systems

Data Converters

Radio Architectures

Networks and Comm.
Systems

Smart Interface



Integrate algorithms in the AMS interface



Research topics

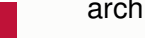
Cognitive Radio Network – Software defined radio

- Algorithms & Architecture
- Game theory based algorithms for security and reliability

Architectures for communication systems

- Rx architecture level : discrete-time receiver, $\Sigma\Delta$ receiver, CS
- ADC architecture : $\Sigma\Delta$, Flash, Time-Interleaved

Circuit-level design and algorithm implementation in CMOS

- ADC: Flash, $\Sigma\Delta$, Time-Interleaved
 - Radio Receiver : $\Sigma\Delta$ receiver, analog discrete-time processing
 - Rx building blocks : filter, AGC, ADC, PLL, etc.
 - Digital algorithm : mismatch correction in time-interleaved architecture, digitally-assisted analog IC
- 



Partnerships

■ Industrial

- Thales
- NXP
- STMicroelectronics
- Lesia
- Technicolor
- Airbus
- LivaNova

■ Academic

- Supelec
- ESIEE
- Polytechnique et ETS Montréal
- Sup'Com Tunis
- Berkeley Wireless Research Center
- Murmann Mixed-Signal Group

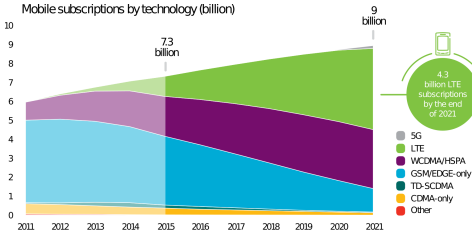
■ Recent research projects

- PANAMA (2010-2013)
- LIFLEX
- CORTIF (Coexistence of RF Transmission in the Future)
- STAR (Smart data for space astrophysical observations)

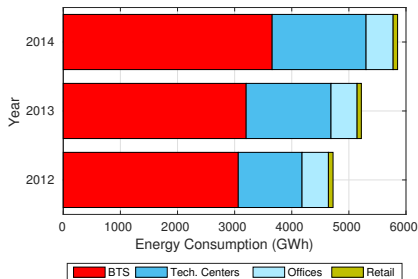
Research context

■ Increasing demand ¹

Mobile subscriptions by technology (billion)



■ Energy consumption ²



■ 5G Network Evolution : IoT

● Requirements

- Larger signal bandwidths
- Low power

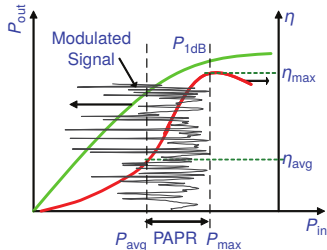
● High level enablers

- Massive MIMO
- cm/mm-Wave bands
- Small cells

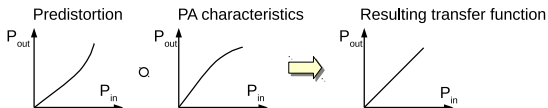
¹ Ericsson Mobility Report 2016 ; ² Vodafone Sustainability Report 2015

Transceiver Power Amplifier Characteristics

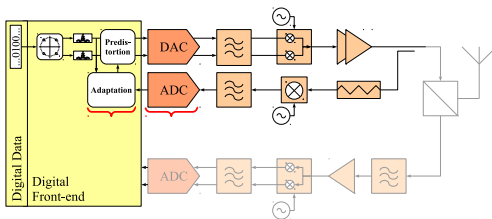
Linearity/efficiency Trade-off³



Fundamental idea

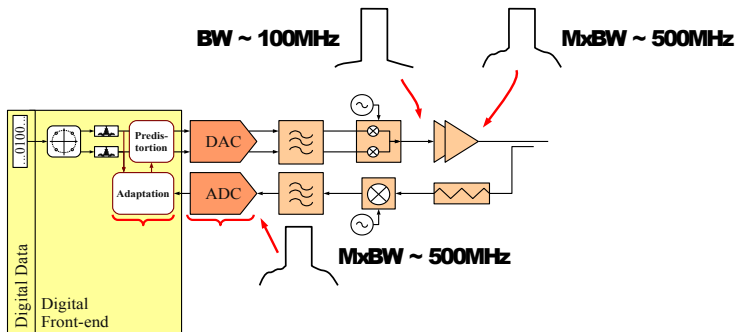


Regular implementation



³ A. Birafane et al. "Analyzing LINC Systems," in IEEE Microwave Magazine, Aug. 2010.

Emerging issues for 5G and small cells



■ RF bandwidth

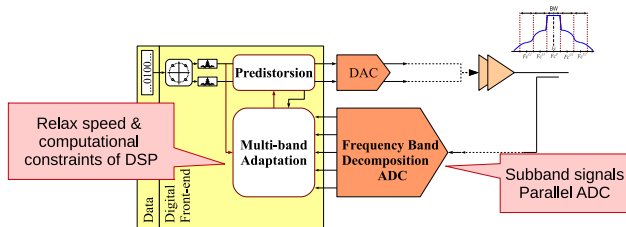
- Feedback path
 - ADC
- Forward path

■ Low power

- DPD identification
- Computation of corrected samples

Proposed approaches

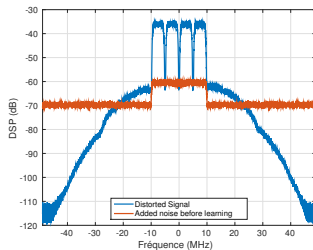
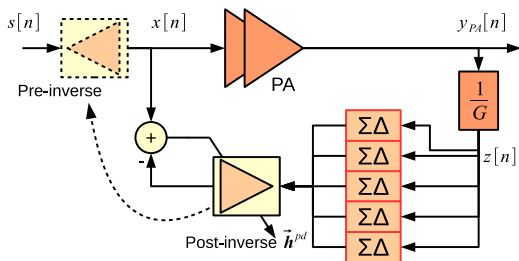
- 5G wideband nodes : joint design of the ADC and DPD architecture
 - Subband ADC
 - Subband multirate digital processing



- 5G low power nodes : Analog RF predistortion
 - DAC rate is relaxed

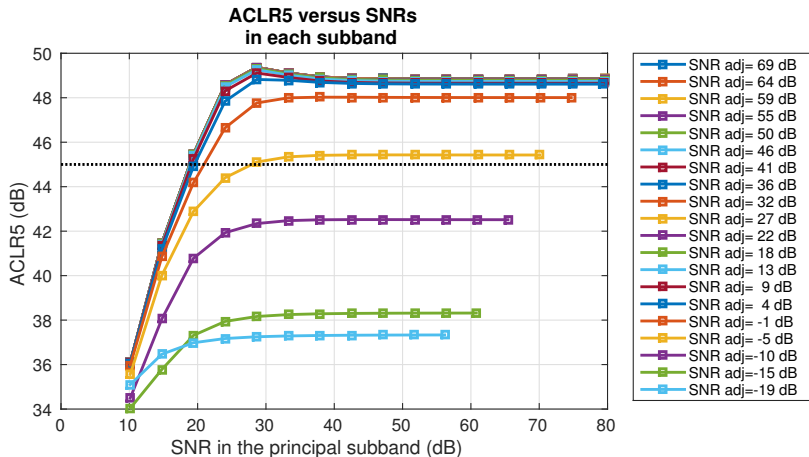
Subband approaches

■ Subband digitization

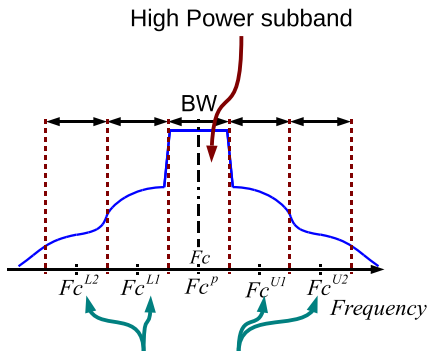


Effects on regular DPD

Effects of independant subband noise levels



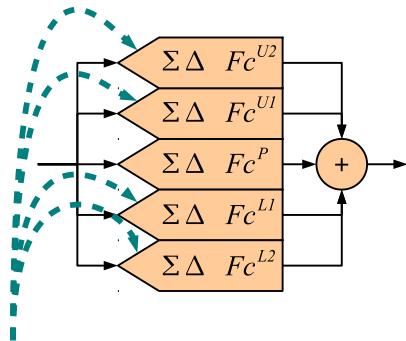
ADC Design challenge



Low Power adjacent subbands

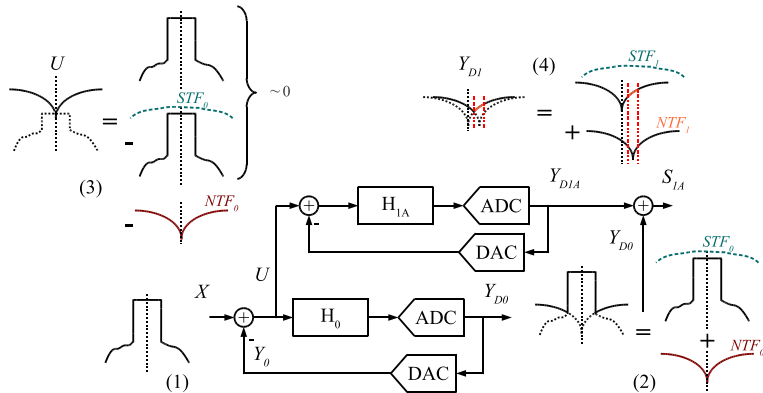
Oversized because of the high power subband

Parallel Subband ADCs



MSNBC $\Sigma\Delta$ Architecture

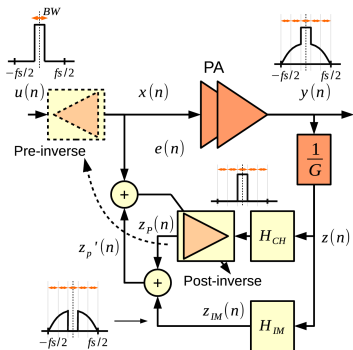
Multi-stage Noise Band Cancellation



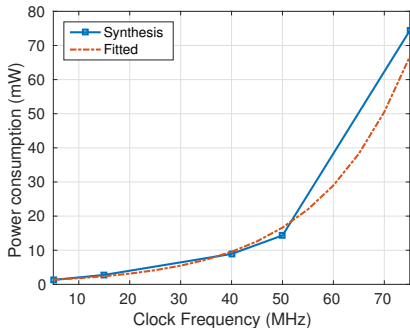
Pham, D.-K.G.; Desgreys, P.; Loumeau, P.; Ridgers, T.; G. Monnerie "High-level design of general multi-stage noise band cancellation $\Sigma\Delta$ ADC optimized for nonlinearly distorted signals," AICSP 2013, Springer

Subband DPD architecture & algorithms

■ Subsampled subband processing



■ Power consumption of ASIC



Pham, D.-K.G.; Gagnon G.; Gagnon F.; Desgreys, P.; Loumeau, P. "Hardware implementation of subsampled adaptive subband digital predistortion algorithm," AICSP 2016, Springer

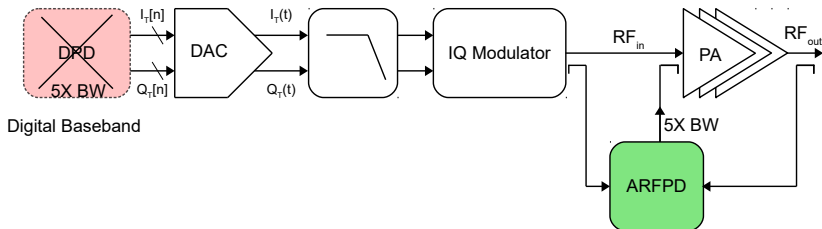


Ongoing and future work on DPD

- ADC design
 - LP Continuous-Time MSNBC
 - 65nm CMOS STMicroelectronics
- Subband architectures
 - Frequency domain processing
 - Multi rate processing

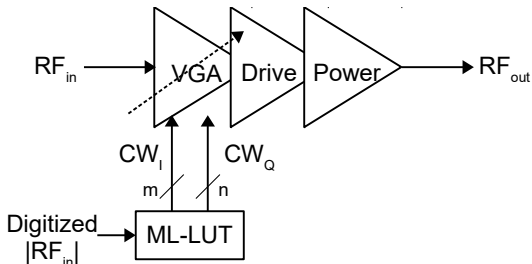
Analog RF Predistorter (ARFPD) - Motivations

- Transmitter signal chain (DAC, filters and IQ modulator) operates at normal signal rate compared to DPD as we predistort just before PA \Rightarrow Lower power consumption!!



Memory-Unaware ARFPD

- ML-LUT in RF domain for handset (UE) application ⁴
- Gain and Phase control using envelope-dependent control words to the first stage (VGA) of PA with vector modulator



- Resulted in increase of linear output power by ~ 2 dBm for WCDMA CMOS UE PA

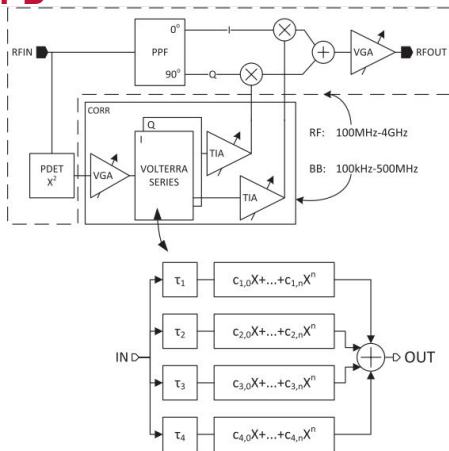
⁴ K. Y. Son, B. Koo, and S. Hong, "A CMOS Power Amplifier With a Built-In RF Predistorter for Handset Applications," IEEE

Memory-Aware ARFPD

- Cancellation of memory terms using simplified Volterra series

$$\sum_{i=0}^{\infty} \sum_{j=0}^{\infty} k_{i,2j+1} X^{2j+1} (\omega t - \tau_i)$$

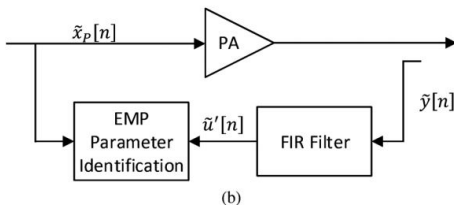
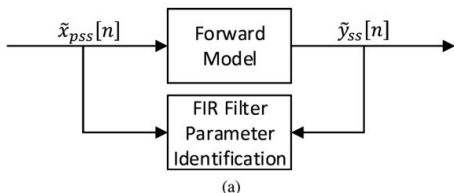
- predistorter IC in 180 nm CMOS with 4th order memory and 11th order nonlinearity consumes 200 mW for 20 MHz BS PA⁵



⁵ F. Roger, "A 200mW 100MHz-to-4GHz 11th-order complex analog memory polynomial predistorter for wireless infrastructure RF amplifiers," in Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International, pp. 94–95, Feb. 2013

Memory-Aware ARFPD with BB FIR filter

- Improvement of at least 3 dB ACPR upto 80 MHz compared to MP using BB FIR filter ARFPD⁶
- Coefficients calculation through SSAPI algorithm
 - PA Forward model estimated
 - Forward model fed with small signal training data
 - FIR coefficients derived
 - EMP model derived using filter output



⁶ H. Huang, A. Islam, J. Xia, P. Levine, and S. Boumaiza, "Linear filter assisted envelope memory polynomial for analog/radio frequency predistortion of power amplifiers," in Microwave Symposium (IMS), 2015 IEEE MTT-S International



Ongoing and Future Work on ARFPD

- Design of predistorter IC for small cell base-station PA
- Novel ARFPD with reduced complexity
- Signal BWs upto 100 MHz
- Frequency coverage upto 6 GHz
- Ways to reduce overall system power consumption
- Partial Digital Programmability and power-scalability

PA measurements and modeling

Measurements and Modeling of ZX60 PA from Mini Circuits

