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Adaptive optics assisted space-ground coherent optical links: ground receiver performance with digital phase-locked loop

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Abstract— Combination of phase modulation with coherent detection for low Earth orbit satellite-to-ground optical links is currently investigated to meet the current high-data-rate increasing demand. On the downlink, the signal carrier undergoes a large Doppler frequency shift which may in turn severely hinders demodulation and information recovery. We present a coherent receiver architecture which combines adaptive optics correction, to mitigate the atmospheric turbulence detrimental effect, with a digital carrier synchronization system. The latter is based on a phase-locked loop which ensures the compensation of the residual frequency shift that remains after preliminary coarse frequency offset correction. We describe the methodology followed to design such a digital phase-locked loop. As an example, we show that the digital PLL is able to compensate a residual frequency mismatch of 300MHz with a convergence time inferior to 1s which is reasonable compared to the duration of the satellite pass.

Keywords—Digital phase-locked loop, coherent, Low Earth Orbit, carrier synchronization, downlink.

I. INTRODUCTION

For both fiber-optics and free-space communication networks, methods using coherent detection which exploit the phase state of the signal provide a better sensitivity and enable the use of higher-order modulation formats as compared to systems based on intensity modulation and direct detection [1][2]. Inter-satellites optical communications links are already operational and their performance improves by using this coherent technique [3][4]. As for the space-ground channel, experimental coherent transmissions have already been established in uplinks and downlinks with geostationary (GEO) and low-Earth-orbit (LEO) satellites [5].

Coherent reception requires that the incoming signal from the satellite be combined with the light from a local oscillator (LO) laser at the ground station. However, coherent receivers are very sensitive to the channel impairments and require accurate carrier/phase synchronization. In particular, the received signal will present a frequency mismatch with respect to the LO due to the Doppler shift and the frequency drift of the satellite laser source. This frequency shift as well as the different phase noises induced by propagation and by

the fluctuations of the laser optical phase will disturb the recovery of the information.

Analog optical phase-locked loops (OPLL) are used to compensate large frequency offsets in inter-satellite data transmissions [6][7]. Optical phase-locked loop coupled with an optical injection loop technique is also proposed for LEO in [8] satellite-to-ground links to compensate frequency mismatch, which was evaluated to be of the order of 9 GHz. Here we assume that the major part of the frequency mismatch is compensated by a preliminary coarse frequency estimation stage, based for example on ephemerides. A residual frequency offset will however remain between the input signal and the local oscillator at the ground receiver. This offset amplitude may go from several dozens to a few hundreds of megahertz. It is the purpose of the present work to address such a residual offset by means of a digital phase-locked loop (DPLL).

The main advantages of DPLL over OPLL are the flexibility and the ease of reconfiguration if the requirements come to change over time. In this paper, we report the results of a preliminary study leading to the design of a DPLL able to compensate frequency shifts of the order of dozens of megahertz or more within a reasonable convergence time. In the present study, as a first step and since the emphasis is placed here on the DPLL design method, the received signal power is assumed to be constant and known. The robustness of the DPLL under more realistic propagation conditions, particularly signal fadings caused by atmospheric turbulence, is investigated in the companion paper [9].

First the overall architecture of the coherent receiver under consideration is presented in part II. Then each element of the DPLL is described in part III. The physical role of the key parameters is emphasized in order to arrive at a design methodology for the system. A design example is presented in part IV supported by simulations results for different initial frequency mismatches.

II. COHERENT RECEIVER ASSISTED BY ADAPTIVE OPTICS

Hereafter in the whole paper, we consider a differentially-encoded optical binary phase shifted keying (BPSK) modulation. At the optical ground station, the received signal is coherently detected by means of intradyne detection. The latter requires that the optical wave be mixed with a LO.

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However, the incoming signal overgoes a frequency shift induced by the Doppler effect. Besides, during the propagation through the atmospheric turbulence, the optical wave undergoes both amplitude and phase degradations. The use of an adaptive optics (AO) system then proves to be essential in compensating for these impairments and maximizing the mixing efficiency [5][10].

After the coherent detection, the signal is sampled by an analog-to-digital converter. Then it is processed by the digital receiver architecture under consideration (see Fig. 1) which consists of an automatic gain control (AGC) loop, a DPLL, a symbol detector and a differential decoder.

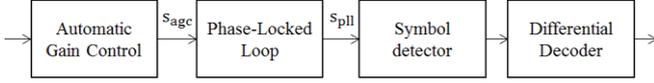


Figure 1. Architecture of the digital carrier synchronization system

An efficient AO system will compensate for a large part of the amplitude fluctuations caused by atmospheric turbulence. However, the residual fluctuations may still hinder not only the mixing efficiency but also the phase detection process within the DPLL. As such they need to be addressed to ensure robust synchronization. This is the role of the automatic gain control (AGC) which aims at maintaining the signal power at the constant target value assumed in the DPLL design (more about this latter). The paper focuses on the compensation of the residual Doppler effects, the additional issue of turbulence is addressed in [9].

We consider that the major part of the frequency mismatch induced by the Doppler effect is pre-compensated by a preliminary coarse frequency estimation stage based for instance on the knowledge of the satellite trajectories. A residual frequency shift still remains, due among other things to the frequency instability of the emitter laser and LO. It is then the role of the DPLL to compensate for this residual frequency mismatch as well as for any additional small phase variation between the data signal from the satellite and the LO. DPLL are a common solution for robust carrier frequency tracking in global navigation system (GNSS) [11]. They offer the advantage of tracking both the frequency shift Δf and the phase variations induced by the atmospheric turbulence.

After the DPLL stage, the BPSK symbols are detected and differentially decoded.

III. DIGITAL PHASE-LOCKED LOOP

The phase-locked loop is here the key element for carrier synchronization. By first assuming an ideal AO and AGC compensation so that the signal power is constant and known, we investigate the feasibility of designing a DPLL adapted that could meet the constraints of our application.

A. Overall description

The loop aims at acquiring and tracking the phase and frequency mismatch between the incoming signal and the local oscillator. Fig. 2 shows the block diagram of the studied DPLL with its three main components: the phase detector, the loop filter and the numerically controlled oscillator (NCO).

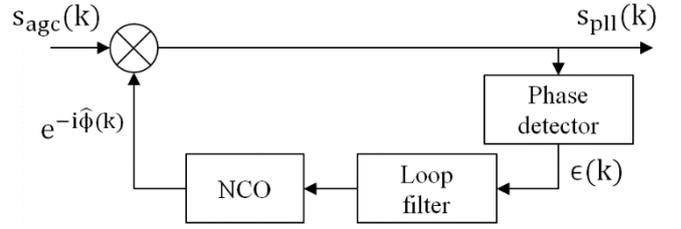


Figure 2. Block diagram of the digital phase-locked loop

First, the signal goes through the following phase detector function which derives from Maximum A Posteriori estimation of an unknown carrier phase offset affecting a BPSK modulated signal, implemented in the form of a closed-loop iterative synchronizer [12]:

$$\epsilon(k) = s_{pll,Q}(k) \tanh(s_{pll,I}(k)) \quad (1)$$

$s_{pll,Q}$ and $s_{pll,I}$ are the real and imaginary parts of the output signal s_{pll} . This estimator is specific to BPSK and does not assume prior knowledge of the transmitted data symbols. Extension to higher-order modulation requires modifying accordingly the phase detector, but apart from that, the proposed design methodology to be described shortly after remains essentially the same.

At low signal-to-noise ratio (SNR), the approximation $\tanh x \approx x$ can be used [12]. An accurate approximation of the phase detector characteristic is then:

$$\epsilon(k) = \frac{K_d}{2} \sin(\phi(k)) \quad (2)$$

The phase error evaluation depends on the phase detector gain K_d which corresponds to the average power of the signal s_{pll} . Both the AO system and the digital AGC reduce the amplitude of the signal fluctuations and thus reinforce the reliability of the PLL by stabilizing the value of K_d . Here, we assume a constant, unitary target signal power so that $K_d=1$. The phase offset $\phi(k) = 2\pi\Delta f k + \varphi(k)$ accounts both for the phase error $\varphi(k)$ and for the frequency offset Δf to be estimated and compensated.

The signal $\epsilon(k)$ is then processed by a second-order loop filter having the following discrete time transfer function:

$$F(z) = K_1 \left(1 + \frac{K_2}{z-1} \right) \quad (3)$$

where K_1 and K_2 are the loop filter gains.

The NCO consists of a first order integrator with discrete time transfer function:

$$H(z) = \frac{K_0}{z-1} \quad (4)$$

where we assume unit gain $K_0=1$.

Finally, the estimated phase error $\hat{\phi}(k)$ is subtracted from the next sample signal phase $s_{AGC}(k+1)$.

B. Design

When working with analog PLL, it is common practice to use intermediate variables to design the loop instead of directly specifying the values for the loop filter gains K_1 and K_2 [13]. Following the same methodology, we consider that the phase error is small enough to linearize the phase detector equation:

$$\epsilon_k = K_d \phi_k \quad (5)$$

It is then possible to identify the damping factor ξ and the normalized natural frequency $\omega_n T$ from the linearized system transfer function, as is commonly done in control theory for a second-order closed loop.

$$\xi = \frac{1}{2} \sqrt{\frac{K}{K_2}} \quad (6)$$

$$\omega_n T = \sqrt{KK_2} \quad (7)$$

where T is the symbol time and $K = K_d K_1 K_2$.

Successfully applying the methods for analog PLL design to digital PLL design requires that the natural frequency ω_n be small compared to the sampling rate [13]. In our design, we thus need to fulfil this condition. The damping factor and the natural frequency are directly related to the stability domain of the loop. The damping factor is commonly chosen in the literature as $\xi = \frac{1}{\sqrt{2}}$ as a trade-off between the loop stability and the convergence speed.

The *hold-in range* is the maximum value of the phase error $|\phi|$ for which the loop is able to converge to a stable equilibrium point. For larger phase errors, the PLL is unstable. Similarly, the *pull-in range* defines the maximum phase jump $|\phi|$ between the incoming signal and the NCO signal that a PLL, starting from a stable state, is able to compensate. The time required by the loop to converge towards a stable equilibrium point and establish the lock is called the pull-in time T_p . By considering a phase error in the form of $\phi(k) = 2\pi\Delta f k + \varphi(k)$, the stable equilibrium points do not depend on the loop parameters for an analog PLL [14]. This means that the *hold-in range* and the *pull-in range* are infinite and that the loop is theoretically able to compensate for any frequency offset, provided the PLL is given enough time to do so. However, in our application, we cannot tolerate an infinite pull-in time, so the parameters need to be carefully chosen to limit this value. The pull-in time may be expressed as a function of the intermediate variables described previously which facilitates the design [13]:

$$T_p = \frac{8(\pi\Delta f)^2}{\xi\omega_n^3} \quad (8)$$

It must also be noted that the values of the *pull-in* and *hold-in range* need to be interpreted with caution in the digital case. Considering a semi-sinusoidal phase detector, if the phase jump between two successive samples exceeds $\pi/2$ then the PLL will no longer be able to accurately track the error and will then become unstable. For example, by considering a loop frequency $f_L = 10\text{GHz}$, corresponding to a DPLL operating at the symbol rate for a 10Gb/s transmission system, the maximum frequency shift Δf (with $\varphi=0$) that can be theoretically compensated is $f_L/4=2.5\text{GHz}$.

The *pull-out frequency* corresponds to the maximum frequency shift between the incoming signal and the NCO signal that the PLL is able to compensate without cycle-slips by returning to the same stable equilibrium point. For an analog loop with a semi-sinusoidal phase detector [14], the absolute value of the *pull-out frequency* is given by:

$$\Omega_{PO} = 1.24\omega_n \left(\frac{1}{\sqrt{2}} + 0.74\xi \right) \quad (9)$$

The value of the pull-out time gives an indicator of the validity of (8). If $\Delta f \ll \Omega_{PO}$, the value of T_p is optimistic for the digital loop.

It is also convenient to define the normalized loop bandwidth $B_L T$ which can be expressed both using the design parameters ξ and $\omega_n T$ or with the different loop gains:

$$B_L T = \frac{\omega_n T}{2} \left(\xi + \frac{1}{4\xi} \right) = \frac{1}{4} (K + K_2) \quad (10)$$

The error signal ϵ described in (2) does not take into account noise. In the presence of additive noise, the signal is impaired by two additional terms involving the products signal \times noise and noise \times noise. For an equivalent analog PLL without phase modulation, the loop performance is lower-bounded by the Cramer-Rao bound (CRB) [12]:

$$\sigma_{\text{CRB}}^2 = \frac{B_L T}{\frac{E_s}{N_0}} \quad (11)$$

For a BPSK modulated signal, an additional penalty is induced on the CRB, the so-called squaring loss (SL) [12]. In this case, the variance of the phase error is approximated by:

$$\sigma_{\text{BPSK}}^2 = \sigma_{\text{CRB}}^2 \times \text{SL} = \frac{B_L T}{\frac{E_s}{N_0}} \times \frac{2 \frac{E_s}{N_0}}{2 \frac{E_s}{N_0} + 1} \quad (12)$$

Fig. 3 represents the phase error variance as a function of the signal-to-noise ratio in a case of a constant amplitude signal impaired by additive white Gaussian noise (AWGN). For two different values of the normalized loop bandwidth product $B_L T=0.005$ and $B_L T=0.0005$, the figure compares the theoretical phase error variance with/without BPSK modulation computed from (11) and (12), respectively, to the corresponding experimental points obtained by simulation. At high enough SNR, the simulated curves superimpose with the theoretical phase error variance for BPSK penalty which is expected. On the other hand, at low SNR, the DPLL is unable to lock. The minimal, critical SNR under which the DPLL becomes unstable depends on the value of the loop bandwidth product $B_L T$. For $B_L T=0.005$, the critical value is $\sim -3\text{dB}$ which is approximately 5dB higher than the critical SNR measured for $B_L T=0.0005$.

The loop bandwidth thus not only impacts the variance of the phase error at the output of the PLL but also the minimum SNR value beyond which the loop is able to lock in.

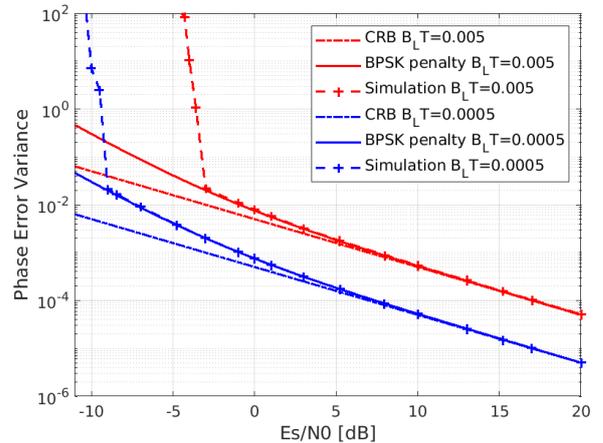


Figure 3. Phase error variance as a function of the SNR E_s/N_0 for normalized loop bandwidths of 0.005 and 0.0005.

Besides if the phase changes abruptly by a multiple of $\pi/2$ because of the noise, the PLL will temporarily lose the synchronization. The probability of those so-called cycle-slips shall be kept as low as possible during the pass of the satellite.

The lower the value of the loop bandwidth, the lower the probability of cycle-slip due to noise [13].

On the other hand, the normalized bandwidth $B_L T$ is also directly related to the convergence speed of the loop. The LEO satellite is only visible for a few minutes. The pull-in time thus needs to be as short as possible to maximize the opportunity for data transmission. For instance, by increasing the loop bandwidth by a factor 10, the acquisition time is reduced by 1000. The loop bandwidth needs to be carefully chosen to ensure lock in a reasonable amount of time and yet limit as much as possible and at the same time the sensitivity to noise during data transmission.

IV. DESIGN EXAMPLE

As our starting point, we adopt a normalized loop bandwidth $B_L T = 0.0005$ to limit the probability of losing synchronization due to noise. In fact, even with residual amplitude fluctuations, we do not expect the system to reach the critical SNR value $E_s/N_0 \approx -8$ dB. With these parameters, the natural frequency is 9.3 MHz which is smaller than the symbol rate of 10 GBaud thus fulfilling the condition ensuring validity of the analog formula in the digital case.

Assuming that the phase detector gain K_d is constant and known (here $K_d=1$) and unit NCO gain ($K_0=1$), the loop filter gains K_1 et K_2 are then completely defined by the value of the loop bandwidth and the damping factor ξ using (6) and (7).

TABLE I. MAIN PARAMETERS OF THE DPLL

Loop frequency f_L	10 GHz
Loop bandwidth B_L	5 MHz
Pull-out frequency Ω_{PO}	14 MHz
Damping factor	$1/\sqrt{2}$
K_1	$1.3 \cdot 10^{-3}$
K_2	$6.7 \cdot 10^{-4}$

In the case of inter-satellites links the residual frequency offset due to the Doppler effect is evaluated to be ~ 30 MHz [15]. We assume that the residual frequency mismatch is of the same order of magnitude and compare the result of our simulations with the expected values obtained using (8) for initial frequency offsets of 30 MHz, 100MHz and 300 MHz, respectively. The pull-out frequency is inferior to the initial frequency shifts, which confirms the validity of (8) to evaluate the pull-in times.

Fig. 3 – 5 show the frequency offset compensation during the acquisition process of the DPLL for the different initial frequency mismatches at a target SNR $E_s/N_0 = 10$ dB.

TABLE II. EXPECTED PULL-IN TIME FOR DIFFERENT INITIAL FREQUENCY OFFSETS

Initial Frequency offset (MHz)	Expected pull-in time (ms)
30	~ 0.12
100	~ 1.4
300	~ 12

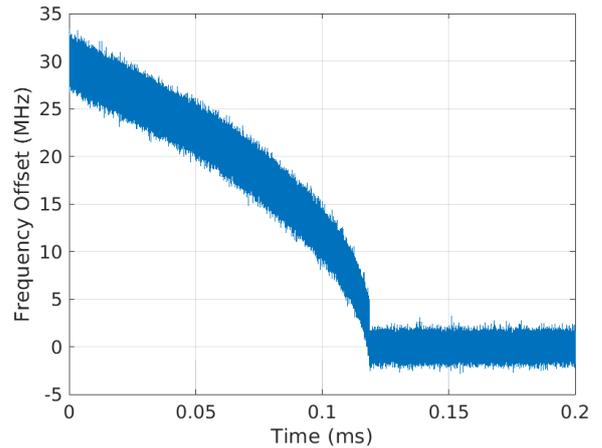


Figure 4. Frequency offset during the acquisition process with an initial frequency mismatch of 30 MHz. $E_s/N_0=10$ dB

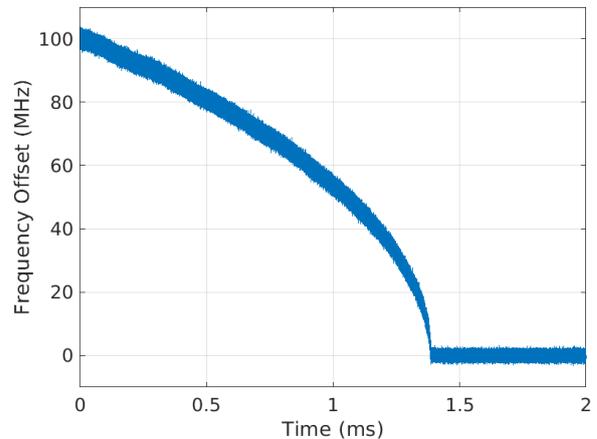


Figure 5. Frequency offset during the acquisition process with an initial frequency mismatch of 100 MHz. $E_s/N_0=10$ dB

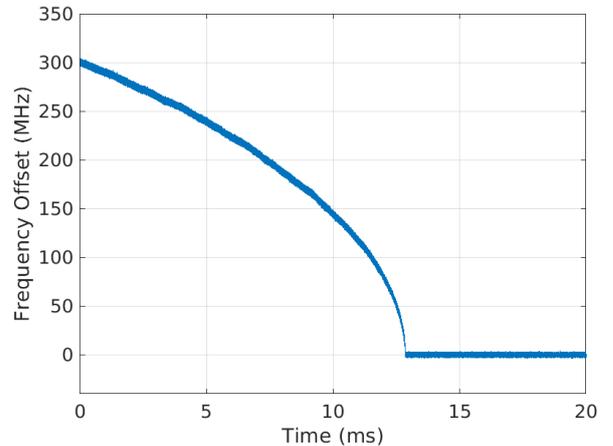


Figure 6. Frequency offset during the acquisition process with an initial frequency mismatch of 300 MHz. $E_s/N_0=10$ dB

The results show that in the three cases the pull-in time calculated with the formula for analog loops gives a good estimation of the actual pull-in time measured by simulation. Besides, for LEO-to-ground applications, acquisition times shorter than 1s seem quite reasonable.

As explained in part III, the pull-in time could be reduced for higher initial offset values by increasing the loop bandwidth, ensuring a SNR higher than the critical value at all time during the satellite pass.

V. CONCLUSION

In the framework of optical coherent LEO-to-ground links, a robust carrier synchronization system is required to correctly recover the transmitted data bits in the presence of satellite Doppler shifts. We propose a coherent receiver composed of an adaptive optics system which maximizes the mixing efficiency between the signal and the LO and a digital carrier recovery stage, based on a DPLL. The design of the DPLL has been described to highlight the role of the loop bandwidth in the convergence speed and in the noise sensitivity of the loop. With proper caution in the design process, the pull-in time can be evaluated in a very simple and accurate manner based on formulas initially derived for analog PLL. The results demonstrate the possibility to design DPLL with a pull-in time shorter than 1s, thereby offering good additional margin against noise.

The whole study was conducted here assuming a constant amplitude signal. However, amplitude variations will remain after the AO system in a practical FSO satellite to earth downlink. The performance of the described digital receiver in the presence of realistic atmospheric turbulence conditions has been investigated in [9].

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