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OxRAM-based Non Volatile Flip-Flop in 28nm FDSOI

N. Jovanović[1,3,4], O. Thomas[1], E. Vianello[1], J-M. Portal[2], B. Nikolić[3], L. Naviner[4]
[1]CEA, LETI, Minatec campus, Grenoble 38054, France, email: natalija.jovanovic@cea.fr
[2]IM2NP, UMR CNRS 6242, Aix-Marseille Université Marseille, France
[3]Dept. of Electrical Engineering and Computer Sciences, University of California, Berkeley 94720, USA
[4]Telecom ParisTech, Paris 75637, France

***Abstract*— This paper presents a robust OxRAM-based non-volatile flip-flop (NVFF) solution, designed for deep nano-scaled CMOS technologies. Forming, set and reset operations rely on a reliable design approach using thin gate oxide CMOS. The NVFF is benchmarked against a standard FF in 28nm CMOS FDSOI. Non-volatility is added with minimal impact on the FF performances.**

I. INTRODUCTION

The new growing area in semiconductor industry is the Internet of Things, which leads to an increased interest in design of Ultra-Low Power (ULP) embedded systems. Apart from the energy efficiency as a main requirement, the important property of these systems is their low activity. For these reasons, they can benefit from including the Non-Volatility (NV) feature in latch based elements, e.g. memories and FF. NV can provide saving the state of the system before going to long zero-consumption sleep mode, while guaranteeing fast sleep/wake-up transitions. Resistive switching memories (ReRAMs) are considered as one of the most promising technologies for future low-cost embedded Non-Volatile Memories (NVM) due to their fast switching behavior, simple CMOS co-integration (compatible materials, BEOL process) and high integration density.

Several Non-Volatile Flip-Flop (NVFF) solutions realized by adding NV devices to the standard master-slave flip-flop (MSFF) are reported [4-6]. Some latch-ReRAM designs [5] are built by connecting NV devices directly or through access transistors to internal nodes of the latch. Therefore, the programming of ReRAM devices is performed using transistors in the latch core and its power supply. When such strategy is applied to the design based on advanced CMOS nodes or ReRAM technology that requires high programming currents/voltages, the size of devices in the latch drastically increases and leads to degraded flip-flop performances and consumption. This approach also requires the increase of latch voltage during the store mode. On the other hand, the design proposed in [6] adds the NV feature with minimal impact on the consumption and performance of the latch in active mode by decoupling programming part from slave latch, and this method is adopted in this work.

Most of the previous NVFF designs are realized with over-130nm CMOS nodes. In this work, using sub-130nm technologies in NVM design is explored. Static consumption which is a weak point of advanced CMOS nodes can be (1) minimized in active mode by using thin-film technologies (FDSOI, FinFET) and (2) completely canceled in the sleep mode due to NVM. In this case the required ReRAM programming voltages may be above the maximum voltage that ensures reliable transistor operation. This is particularly true for the electroforming of fresh ReRAM devices that requires higher voltage (between 2.5V and 5V) than SET/RESET operations. The use of such high voltages can lead to an oxide breakdown or reduce device lifetime. In over-130nm nodes the exposure of transistors to high stress can be minimized by dynamically changing the power supply [6]. This approach becomes ever more limited as technology scales below 130nm node due to an increasing voltage gap between ReRAM and CMOS.

This paper presents a robust and reliable NVFF implemented with oxide-based ReRAM (OxRAM) and 28nm CMOS FDSOI technologies. It is realized using only thin gate oxide transistors as regular standard cells. Moreover, it implements a simple and reliable forming solution. Speed and power consumption analyses are performed and the solution is compared to a standard FF cell. The reminder of this paper is organized as follows. Section II introduces used ReRAM technology. Section III explains the proposed solution and section IV is dedicated to results and discussion.

II. RERAM TECHNOLOGIES

a) Technology background

ReRAM operation mechanism is based on the resistance change in an active material, usually a transition metal oxide sandwiched between two metal electrodes [1].

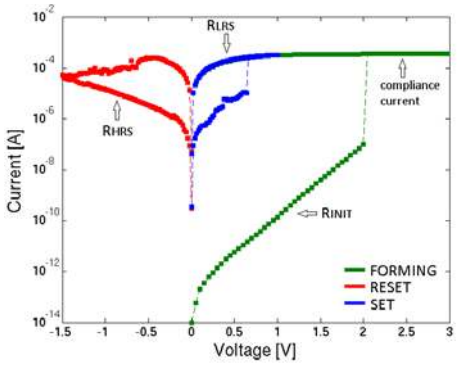

Fig. 1. Quasi-static I-V characteristics obtained from experimental data.

The TiN(35nm)/HfO_2(5nm)/Ti(10nm) resistor is a promising OxRAM stack in terms of operating voltages and reliability [2, 3]. The typical device quasi-static characteristic is shown in Fig. 1. A pristine memory device that is in the high initial resistance state can be switched to the low resistance state by applying a high voltage stress (green). This process is called forming and it alters the resistance of the pristine device irreversibly. After the forming step, the RESET (red) and SET

(blue) occur in the opposite polarity. A switching time of 100ns, data retention up to 68 days at 150°C and a high endurance up to 10^8 cycles is achieved.

b) Electrical characterization

The experimental data obtained on this technology are used for calibration of the compact model that is used in the following Sections [8].

OxRAM and CMOS co-integration is deeper explored by simulating Transmission-Gate + OxRAM configuration ($w_p = 1.6 \cdot w_n$). Fig. 2 depicts the relation between SET and RESET parameters (t_{SET}, t_{RESET}, V_{SET} and V_{RESET}) and their behavior in differently sized configurations. SET switching time is defined as the time it takes for device resistance to decrease from initial R_{OFF} value to R_{ON}=2kOhm. RESET switching time is defined as the time it takes for current through the device to decrease from initial value (when R_{ON} = 2kOhm) to a stable value. In each test, same voltage (V_{SET}/V_{RESET}) is applied across the whole structure and on the transistor gates, in accordance with timing diagrams for SET and RESET operations depicted in the inset of Fig. 2.

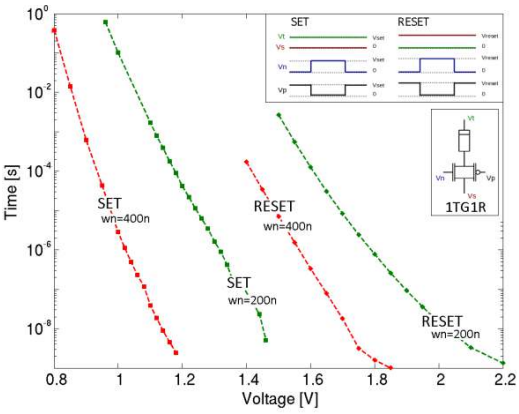

Fig. 2. 1TG1R structure: t_{SET} vs V_{SET} and t_{RESET} vs V_{RESET} for w_n = 400nm (red) and w_n = 200nm (green).

These results highlight exponential time-voltage dependencies and show that SET and RESET conditions are different. Moreover, the structure with larger access transistors requires smaller voltages for same switching times – property which can be used to overcome the gap between different SET/RESET conditions. Finally, these data show the need for high voltages in the design. Even with enlarged transistors, V_{RESET} will be above the CMOS operating range if fast switching behavior is targeted (e.g. 1.7V for 10ns reset of 1TG1R structure with w_n=400nm). This is particularly true for forming operation, as it typically requires increased voltages (Fig. 1), even without taking the operation speed into consideration. This property of OxRAM technology introduces reliability concerns when co-integrating 28nm FDSOI and OxRAM technologies.

III. Proposed Solution

a) Working principle

NVFF is realized by adding OxRAM devices in the slave stage of MSFF. All NV operations are performed while clock is low, i.e. when master passes the input value while slave is disconnected from the master and holds previous data. During regular FF operations (*active mode*) NVM block is disconnected. During data-backup information from flip-flop is transferred to NVM (*store*) which is followed by the system going to *sleep mode* (power off). After switching the power on, slave latch will asynchronously recover previously saved content (*restore*).

Block diagram of implemented solution is given in Fig. 3. Two different power supplies are used in the cell - VddH (yellow blocks) and Vdd (blue). NVFF_CORE is MSFF that is modified by adding: (1) inverters that provide *Q_s* and *Qb_s* which are used for store operation, and (2) header and equalizer transistors used for restore operation. Signals *Q_s* and *Qb_s* are combined with *STORE* signal in the logic block, and the voltage levels of obtained signals *A*, *Ab*, *B* and *Bb* are shifted in two level-shifter (LS) blocks and brought to NVM part where they are used to control the store operation. The level-shifted *FORM* signal is used in NVM during forming operation and *RESTORE* and *ActRest* are responsible for the NVM behavior in active and restore modes. All components are explained in further parts of this section.

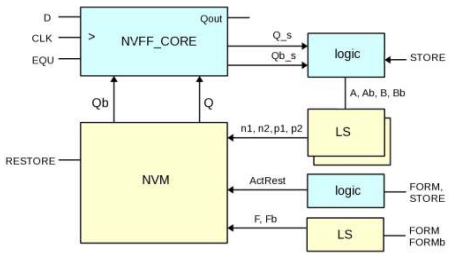

Fig. 3. Block diagram of implemented NVFF

b) NVM and logic blocks

NVM part employs two OxRAMs (Fig 4). Each device has different paths assigned for store (red for SET and green for RESET), forming (blue) and active/restore modes (pink).

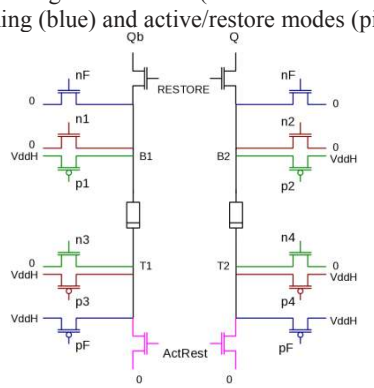

Fig. 4. NVM part – principle

Control signals *n1 – n4*, *p1 – p4*, *nF*, *pF* and *ActRest* are generated according to Table I. During store mode SET operation on one OxRAM and RESET operation on another one are performed in parallel, in accordance with *Q* value. The resistance difference is sensed during restore mode. FORMING step is performed simultaneously on both devices,

regardless of the value of Q. During active and restore modes top electrodes of both OxRAMs are grounded. In order to accomplish specified operation modes functions (1) - (4) are realized in logic blocks.

TABLE I. CONTROL SIGNALS FOR NVM PART

mode	bottom electrodes	top electrodes	forming	*ActRest*
FORMING	p - off n - X	n - off p – X	**p, n – ON**	n - off
ACTIVE RESTORE	p, n - off	p - off n - X	p, n - off	**n -ON**
STORE	**$n_1 = p_1 = Q$** **$n_2 = p_2 = Qb$**	**$n_3 = p_3 = Qb$** **$n_4 = p_4 = Q$**	p, n - off	n - off

$$p_2 = p_3 = \overline{n_1} = \overline{n_4} = A = \overline{\overline{FORM} \cdot Q \cdot STORE} \quad (1)$$
$$p_1 = p_4 = \overline{n_2} = \overline{n_3} = B = \overline{\overline{FORM} \cdot \overline{Q} \cdot STORE} \quad (2)$$
$$n_F = \overline{p_F} = FORM \quad (3)$$
$$ActRest = \overline{FORM + STORE} \quad (4)$$

c) Reliability issues

The difference between OxRAM programming voltages (VddH in NVM block) and CMOS operating voltages (Vdd in logic blocks) imposes inserting level-shifters between these parts. In order to ensure reliable operation for all transistors in the critical paths, they are cascoded and biased in a way that guarantees limited voltages across the terminals of every stacked transistor.

Fig. 5 depicts the solution used in implemented NVFF cell. The level shifter [7] with output inverters is generating *inb_H* and *inb_L* signals in appropriate ranges - [VddM, VddH] and [0, VddM], respectively. VddM is an intermediate voltage level chosen such that all pin-to-pin voltages are within the safe operating boundaries. These signals drive the gates of output stage, allowing the *out* signal to vary within [0, VddH].

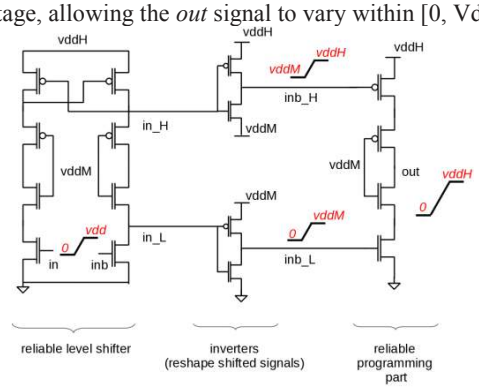

Fig. 5. Reliable programming part and level-shifters – principle.

This method is applied to the store/forming parts of NVM block. Transistors on the right side of Fig.5 correspond to programming transistors in NVM block, with the node *out* connected to OxRAM electrodes B_i and Ti. Functionally, signals *inb_H* and *inb_L* correspond to control signals n_i and p_i realized in logic blocks, but they must be placed in the suitable voltage range – p_i signals in [VddM, VddH] and n_i in [0, VddM]. Hence, level-shifter inputs *in* and *inb* correspond to outputs of logic blocks - signals *A*, *B*, *FORM* and their inverted values. Although SET and FORMING paths are separated, cascode transistors can be shared between them. This solution requires additional power supply VddM that is chosen to be $\frac{vddH}{2}$ because of the circuit symmetry. NVM block also contains restore/active paths, but they exploit only NMOS transistors which don't need level-shifting. In these parts transistors are also stacked but due to simpler layout $vddM = vdd$ is chosen.

d) Implementation

Detailed schematic of implemented cell is given on Fig. 6. Programming transistors are implemented using low-Vth threshold devices (orange) in order to reduce the area of the cell. The level shifter which generates forming control signals *F* and *Fb* (green) can be shared between the cells in case of integrating multiple NVFF cells in a complex system.

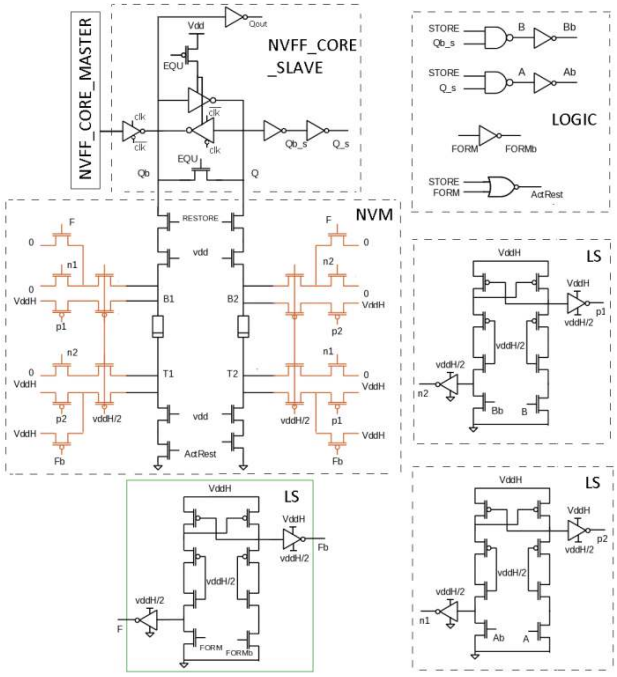

Fig. 6. Implemented NVFF.

IV. RESULTS AND DISCUSSION

Presented NVFF cell is simulated using a 28nm CMOS FDSOI technology and OxRAM model. The circuit is supplied with Vdd=1V and VddH=2.6V(forming)/1.8V(after-forming). Pulses of 70ns (store) and 6ns (restore) are applied. Successful store and restore operations are confirmed with the yield of 99.7% by performing 10000-sample Monte Carlo simulation that takes into account both OxRAM and CMOS local process variations (TT corner, 27°C). The impact of adding NV property to the flip-flop is explored - the performance and power consumption of NVFF are compared to standard MSFF.

a) Performance in active mode

Table II summarizes the timing parameters of NVFF and FF cells. Clk-Q delay, setup and hold times for low-to-high and high-to–low transitions are estimated for both cells under the same conditions (same data and clock slope and output

load). The Clk-Q delay is measured from 40% of clock edge to 60% (LH) or 40% (HL) of the output signal. Setup and hold times are defined as D-Clk delays that cause 10% increase in the Clk-Q delay from its nominal value. The obtained data show less than 4% increase of Clk-Q delay in NVFF case and no difference in setup and hold times.

TABLE II. THE TIMING PERFORMANCE OF NVFF AND FF

	LH			HL		
	t_{clk-q}	t_{setup}	t_{hold}	t_{clk-q}	t_{setup}	t_{hold}
NVFF	30.3ps	14.4ps	-23.7ps	26.8ps	39.5ps	-10.8ps
FF	29.6ps	14.4ps	-23.9ps	25.8ps	39.5ps	-10.8ps

b) Energy in standby mode

During the sleep mode, the power supply for NVFF cell is turned off (Vdd = VddH = 0) resulting in zero leakage. The cell only consumes power before going to standby (store) and after wake-up (restore). Therefore, the energy is independent of the time spent in sleep mode and can be calculated as:

$$E_{sleep_NVFF} = E_{store} + E_{restore} \quad (5)$$

In FF case, supply must retain, but can be minimized to Vmin:

$$E_{sleep_FF}(t_{sleep}, V_{min}) = \int_{t_sleep} V_{min} \cdot I(t) \cdot dt \quad (6)$$

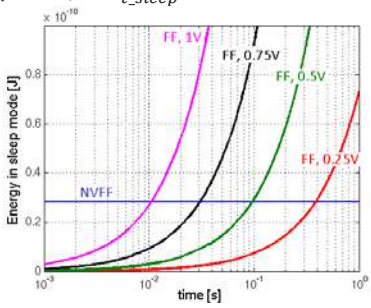

Fig. 7. Sleep mode energy for NVFF and FF supplied with different voltages

Fig. 7 represents E_{sleep_NVFF} and E_{sleep_FF} as a function of the time spent in sleep mode. E_{sleep_FF} is estimated for different supply voltages. NVFF consumes 28pJ for store operation, while restore is not critical and takes less than 0.5% of total energy. For example, if the supply of FF is lowered to 0.5V in sleep mode, replacing it with NVFF solution will reduce the consumption if periods of inactivity are longer than 0.1s.

c) Energy in active mode

The energy consumption of active mode is estimated per clock period during which new data is captured. This value consists of dynamic part that is constant (write to flip-flop) and static part that depends on the clock period, so we calculated the energy for several frequencies. The equation used for FF is:

$$E_{act_FF}(f) = \int_{T_{clk}} Vdd \cdot I(t) \cdot dt \quad (7)$$

For NVFF cell the consumption in NVM and LS blocks that are supplied by VddH is separated from consumption in NVFF_CORE and LOGIC blocks that are supplied by Vdd:

$$E_{act_NVFF}(f) = E_{act_NVFF_Vdd}(f) + E_{act_NVFF_VddH}(f) \quad (8)$$

Fig. 8(a) shows the ratio of active energy in Vdd part of NVFF and active energy in FF cell. Using non-volatile cell increases consumption for 32-37% for the frequency range of 10MHz-1GHz. The difference comes from the modification in slave latch (inverters for *Q_s* and *Qb_s*) and the logic block. It is notable that the difference is higher for lower frequencies, where the leakage becomes dominant to the write energy.

The active energy in VddH part of NVFF is shown on Fig. 8(b) and compared to the active energy in Vdd part of NVFF. Due to the use of large low-Vth devices, high supply voltage of programming part, as well as the presence of three level shifters, the consumption increases drastically, especially for low frequencies. This can be avoided by turning off VddH supply and deactivating NVM/LS part during the active mode.

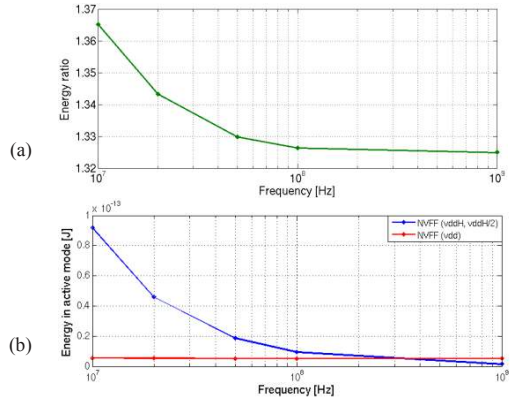

Fig. 8. Energy consumption in active mode: (a) $E_{act_NVFF_Vdd}$ / E_{act_FF} ratio; (b) $E_{act_NVFF_VddH}$ and $E_{act_NVFF_Vdd}$.

V. CONCLUSION

OxRAM–based Non-Volatile Flip-Flop in 28nm CMOS FDSOI technology is implemented and validated. Proposed solution successfully solves the problem of reliability, which is a main issue encountered in co-design of ReRAM and advanced CMOS nodes. Implemented cell is benchmarked against standard MSFF and exhibited a minimal difference in performance. Energy saving in the sleep mode is estimated, and proved to be significant for long inactivity periods. The energy in active mode is increased, but that impact is minimized by disconnecting the NV part during active periods.

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