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PSEUDORANDOMLY CONTROLLED ADC CHARACTERIZATION TOWARDS MULTISTANDARD RECEIVER

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ABSTRACT

The radio communication tendency is to reach Software Radio applied to multistandard receiver. Non uniform sampling controlling Analog-to-Digital Converter in Homodyne multistandard receiver was previously proposed in our works. Non uniform sampling offers the advantage of alias-free sampling. This can lead to many advantages in the multistandard based non uniform sampling receiver such as, essentially, relaxing anti-aliasing filter and reducing power consumption of the analog-to-digital converter. In this paper, we present a pseudo-random signal sampler to control the analog-to-digital converter. This circuit consumes less than the difference between the non uniform sampling and the uniform over-sampling. A complete test setup with instrumentation and spectral analysis will be presented to illustrate alias-free processing measurement.

Index Terms— Radio communication, Signal sampling, Signal reconstruction, Analog-digital conversion, Clocks.

1. INTRODUCTION

With the continuous increase of the number of standards, the challenge is to realize a multistandard software defined radio receiver. Such a receiver ought to be low cost, low power and use highly integrated devices. Our previous works propose to control non uniformly the Analog-to-Digital Converter (ADC) in homodyne receiver [1]. The problem is to generate a non uniform clock with a low power consumption, low area and high frequencies to adapt our work to SDR multistandard receiver.

We proposed in previous work an initial solution to generate a non uniform clock [2]. In this paper, an enhanced solution is proposed, Pseudorandom Signal Sampler (PSS). Implementation and synthesis were done on FPGA and 65 nm CMOS digital technology. A test setup platform is prepared to compare reconstruction and analysis in uniform and non uniform sampling cases.

This paper is organized as following. The second section presents suitable cases for using Non Uniform Sampling (NUS) to verify anti-aliasing sampling. In the third section, we present the multistandard NUS-based homodyne receiver and its advantages. A state-of-the-art of commercial available ADCs is also presented to choose the suitable ADC to the proposed receiver

architecture and to identify its power consumption. In section IV, we propose pseudorandom signal sampler circuit design. In section V, we focus on the PSS circuit implementations on FPGA and ASIC targets. We evaluate maximum frequency, dynamic power consumption and area of the PSS circuit. Then, we realize a test platform to compare spectrum analysis in non uniform sampling and uniform sampling cases. Finally, conclusions and perspectives of this work are outlined.

2. ANTI-ALIASING SAMPLING

Non uniform sampling has a particular advantage which is the anti-aliasing characteristic under some conditions. Instead of the uniform sampling instants $\{kT_s, 0 \leq k \leq N\}$, assume the non uniform sampling instants $\{t_k, 0 \leq k \leq N\}$ with $E[t_k] = kT_s$. The instants $\{t_k\}$ defined by a probability density function $p_k(t)$, have to satisfy stationary condition introduced by Bilinskis [3] and given by (1).

$$p(t) = \sum_{k=0}^{+\infty} p_k(t) = \frac{1}{T_s} \quad (1)$$

with T_s considered as the mean sampling period.

Some non uniform sampling schemes such Jittered Random Sampling (JRS) and Additive Random Sampling (ARS) satisfy this condition. In case of implementation, it is advised to use Time-Quantized Random Sampling applied to the ARS or JRS scheme. A summary of suitable sequences is drawn in Table 1. We define $p_\tau(t)$ as the probability density function of independent and identically distributed variables τ_k with a variance σ^2 . The mean of τ_k is zero for JRS scheme and T_s for ARS scheme. In JRS scheme, only uniform distribution is valid with a statistical parameter σ/T_s equal to 0.2887.

One more adapted scheme to implementation is the pseudorandom version of the TQ-RS scheme. Figure 1 illustrates the Time Quantized PseudoRandom Sampling (TQ-PRS) scheme. In fact, each random instant t_k is replaced by the nearest quantized instant $t_{k,q}$. Each instant $t_{k,q}$ is a multiple of a step Δ with Δ equal to T_s/q_T and q_T is the quantization time factor. The rank n , in the k^{th} interval, is a pseudorandom number with a cycle length q_T .

Table 1. Suitable sequences for anti-aliasing sampling.

Scheme	t_k	$E[t_k], \text{Var}[t_k]$	$p_\tau(t)$	σ/T_s
JRS	$t_k = kT_s + \tau_k$ $E[\tau_k] = 0$ $\text{Var}[\tau_k] = \sigma^2$	kT_s, σ^2	Uniform	$= 0.2887$
ARS	$t_k = t_{k-1} + \tau_k$ $E[\tau_k] = T_s$ $\text{Var}[\tau_k] = \sigma^2$	$kT_s, k\sigma^2$	Uniform Gaussian	≤ 0.2887
TQ-RS	$\delta t_k = t_k - t_{k-1}$ $\delta t_{k,q} = n\Delta$ if $(n-1/2)\Delta < \delta t_k \leq (n+1/2)\Delta$	Same as JRS or ARS scheme		

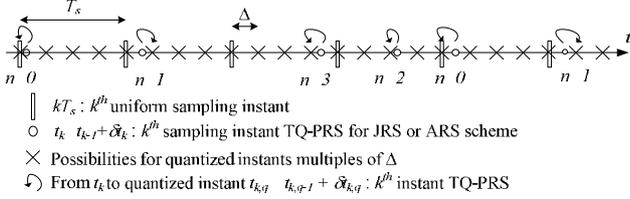


Figure 1. TQ-PRS scheme description for $q_T = 4$.

The TQ-PRS scheme is a kind of implicit over-sampling technique with some restrictions. In uniform sampling, in the spectrum band $[0, q_T f_s]$, aliases are located at frequencies $q_T f_s - f_c$ and $k f_s \pm f_c$ for k between 1 and $(q_T - 1)$ where f_c is the carrier frequency of the sampled signal and f_s the mean sampling frequency equal to $1/T_s$. When we non uniformly sample with TQ-PRS scheme, we obtain only one alias at a frequency equal to $q_T f_s - f_c$. However, some wideband noise replaces the other aliases. This wideband noise could be suppressed with a reconstruction algorithm [1, 4].

3. MULTISTANDARD NUS-BASED HOMODYNE RECEIVER

Homodyne architecture is the most adapted for multistandard receiver. In fact, this architecture offers to use a number of discrete components lower than in the other conventional receiver architectures. Homodyne receiver suffers from some drawbacks as DC-offset and I/Q mismatch. All of these are corrected digitally in DSP as explained in [5]. We propose in previous work to non uniformly control the Analog-to-Digital Converter [1].

As presented in Figure 2, the homodyne architecture is composed of an RF switch to select the suitable RF filter for the standard received and a multiband LNA to amplify the received signal with a low added noise [6].

In previous work [1], we explain how to benefit from the anti-aliasing advantage of the non uniform sampling. In Figure 2, comparing the parts (a) for conventional baseband receiver and (b) for NUS based baseband receiver, we use a relaxed Anti-Aliasing Filter (AAF), we move out, or at least relax, the Automatic gain control (AGC), we replace the clock controlling the ADC by a non uniform clock and we add a digital Reconstruction Algorithm in the DSP.

Relaxing AAF is obtained thanks to the TQ-PRS scheme and its implicit over-sampling characteristic as explained in previous section. Consequently, for instance, we use a

3rd order AAF as in the uniform over-sampling case instead of a large order AAF in sampling case at Nyquist frequency. The IEEE802.11a characterizes the choice of the sampling frequency. When using a 40 dB dynamic AGC, a 10-bit ADC in case of uniform over-sampling at 265.6 MHz is required. This required ADC would be power-hungry, as mentioned in Figure 3 showing ADC power consumption, as stated by the manufacturer, versus resolution and sampling frequency.

Therefore, we propose non uniform sampling technique to also benefit from decreasing ADC dynamic power consumption versus sampling frequency. We ought to use a 10-bit ADC with mean sampling frequency f_s at 16.6 MHz. These results are taken in case of quantization time factor q_T equal to 16. In spite of these advantages, we need to replace the uniform clock CLK controlling the ADC by a non uniform clock CLK_NUS.

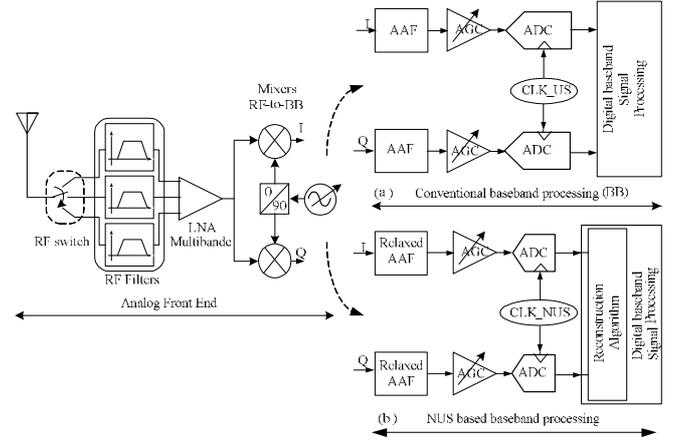


Figure 2. Multistandard Homodyne Receiver (a) Conventional baseband processing (b) NUS-based baseband processing.

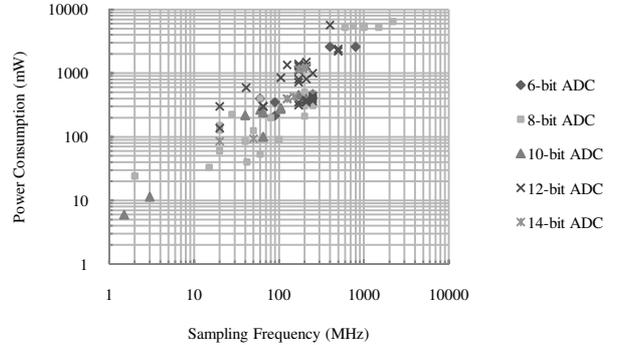


Figure 3. State-of-the-art of commercially available ADC.

4. PSEUDORANDOM SIGNAL SAMPLER CIRCUIT DESIGN

According to TQ-RS scheme, non uniform sampling instants occur at quantized values equal to a multiple of Δ . This quantization can be obtained if we first use a Δ delay block to generate q_T phases $\{\Phi_0, \Phi_1, \dots, \Phi_{q_T-1}\}$ where Δ is the minimum spacing defined by T_s/q_T . Then, the Linear Feedback Shift Register (LFSR) returns pseudorandom numbers $i(m-1:0)$ taken in the set of $\{1, \dots, q_T\}$ at the Φ_0 rate ($1/T_s$). The obtained numbers perform a uniform probability density in accordance to

the JRS scheme because each generated number is taken independently from the previous one as JRS scheme is defined in Table 1.

The drawback of this solution is the overlap between phases in $\{\Phi_1, \dots, \Phi_{(q_T/2)-1}\}$ and phases in $\{\Phi_{q_T/2}, \dots, \Phi_{q_T-1}\}$. We propose a new design, first introduced in [2], called Pseudorandom Signal Sampler (PSS) to overcome overlap problem. Figure 4 illustrates the digital architecture and building blocks of PSS. To produce convenient $\{\Phi_0, \Phi_1, \dots, \Phi_{q_T-1}\}$ for pseudorandom clock generation without overlap, we combine signals $G(m-1:0)$ delivered by the Gray counter at the main clock rate ($f_{clk} = 1/\Delta$). Indeed, the Gray counter stage reduces the number of jumps between delivered signals, and therefore glitches are reduced in the following stages. The $\{\Phi_0, \Phi_1, \dots, \Phi_{q_T-1}\}$ duty cycles are now different from each other and avoid the overlap.

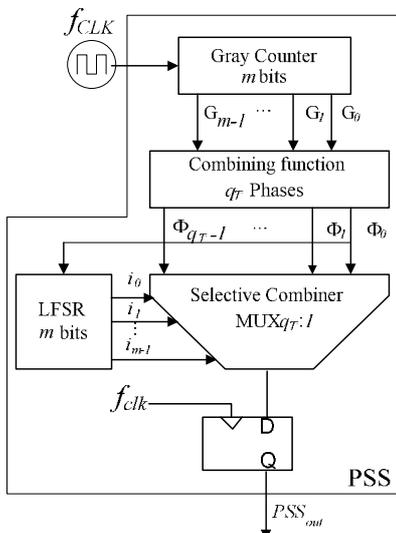


Figure 4. Description of the PSS.

The selective combiner stage, a multiplexer MUX $q_T:1$, selects the phase Φ_i addressed by the generated pseudorandom number i each period of Φ_0 . The multiplexer. However, the multiplexer introduces some delay and its output presents some glitches which are shorter than the specified minimum spacing Δ . For that reason, the multiplexer output is fed through a D-latch controlled by the main clock f_{CLK} to suppress glitches and deliver pseudorandom clock PSS_{out} . The main clock f_{CLK} has a period equal Δ needed for the TQ-PRS scheme as described in Table 1 and Figure 1. The obtained statistical parameter σ/T_s is given in (2).

$$\frac{\sigma}{T_s} = \frac{1}{q_T} \sqrt{\frac{(q_T - 1)^2 - 1}{12}} \quad (2)$$

The "mean" sampling frequency is $f_s = f_{CLK}/q_T$. According to the proposed PSS design, we define the instantaneous pulsewidth, number of Δ occurrences, given in (3).

$$T_i = T_s + \Delta(i(k+1) - i(k)), 1 \leq k \leq q_T - 1 \quad (3)$$

where $i(k)$ is the current LFSR output value. In the case of $q_T = 16$, instantaneous sampling frequency f_i , equal to $1/T_i$, takes values between $f_{smin} = f_{CLK}/24$ and $f_{smax} = f_{CLK}/9$. ADC should be able to convert at all these rates to deliver data at f_s which decreases its dynamic power consumption. In fact, generated frequencies should satisfy (4).

$$f_{smin} \geq f_{Nyquist} \text{ and } f_{smax} \leq 2ERBW \quad (4)$$

with $f_{Nyquist}$ is minimum frequency defined by Shannon theorem to avoid overlap between signal and aliases. Consequently, instead of mean sampling frequency equal to 16.6 MHz, we need to choose f_s at 24.9 MHz to make the minimum sampling frequency, $f_{CLK}/24$, satisfy the Shannon theorem and be at least equal to the IEEE802.11a channel bandwidth.

The signal PSS_{out} is applied to the ADC at $ENCODE$ input to convert the analog signal A_{in} to n-bit resolution digital signal D . ADC timing diagram, in Figure 5, presents timing parameters [7]. An accurate analog-to-digital conversion is only achieved if the PSS_{out} pulsewidth high is higher than the $ENCODE$ pulsewidth high t_{EH} and the PSS_{out} pulsewidth low is higher than the $ENCODE$ pulsewidth low t_{EL} . Therefore, we propose (5) to verify these conditions.

$$DC_i \cdot T_i > t_{EH} \text{ and } (1 - DC_i) \cdot T_i > t_{EL} \quad (5)$$

where DC_i , as we define in (6), is the duty cycle of the signal PSS_{out} relative to the current LFSR output value $i(k)$.

$$DC_i = \frac{T_s - \Delta \max\left(i(k), \frac{q_T}{2}\right)}{T_i}, 1 \leq k \leq q_T - 1 \quad (6)$$

Moreover, aperture delay t_A , clock jitter, output valid time t_V and output propagation delay t_{PD} have to be lower than the minimum spacing Δ as defined by (7).

$$\max(t_A, Jitter, t_V, t_{PD}) < \Delta \quad (7)$$

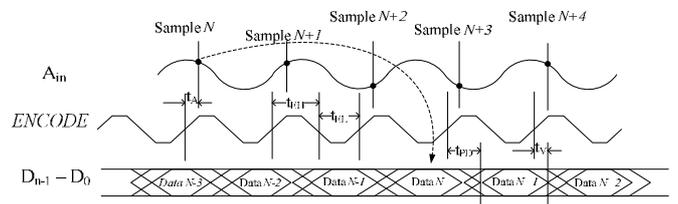


Figure 5. Timing Diagram.

5. TEST SETUP AND MEASUREMENT

5.1. PSS Validation

Functional verification of the proposed PSS architecture is synthesized in VHDL to generate a non uniform sampling clock from a main clock at $f_{CLK} = 420 \text{ MHz}$. The target

FPGA device is EP2C35F672C6 from Altera. The maximum value for mean sampling frequency for q_T equal to 8, 16 and 32 are respectively 13.125 MHz, 26.25 MHz and 52.5 MHz. The obtained statistical parameter σ/T_s is near to the theoretical values, computed from (2), as presented in Table 2. Errors comparing those values with $\sigma/T_s = 0.2887$ required value are 13.4 %, 6.5 % and 3.2 % respectively for q_T equal to 8, 16 and 32.

Table 2. Theoretical and synthesis results for statistical parameter σ/T_s .

	Theoretical results	Simulation results	Errors vs $\sigma/T_s = 0.2887$
$q_T = 8$	0.25	0.2503	13.4 %
$q_T = 16$	0.27	0.2703	6.5 %
$q_T = 32$	0.2795	0.2796	3.2 %

According to the results in Table 2 and to validate proposed idea for circuit design, we choose to implement the PSS architecture, described in the previous section for q_T equal to 16, in CADENCE for a 65 nm digital CMOS technology. The signal generation as described above has been verified through electrical post-layout simulation. PSS occupies a 470 (μm)² die area. It allows a mean sampling frequency up to 200 MHz. PSS circuit consumes between 1.21 μA and 242 μA from 1.2V supply for obtained frequency test between 1 MHz and

200 MHz. These frequencies are obtained when using a main clock frequency between 16 MHz and 3.2 GHz.

5.2. Acquisition Methods

Before analyzing ADC output, we need to adapt available acquisition methods to the non uniform sampling. The viable methods are the acquisition based on data storage in a FIFO [8] and the acquisition based on logic analyzer. Both of these methods are driven by the main clock of the PSS. Then, we follow the processing with a cubic spline reconstruction algorithm on DSP (Digital Signal Processing).

The received data is composed of binary PSS output and 10-bit ADC output. In both acquisition methods, we extract sampling instants and convert ADC output to decimal data. The obtained results are presented in Figure 6.

The test setup is presented in Figure 7 and is described as follows:

- A clock generator delivers the main clock to the PSS implementation on the FPGA device. External clock generator could be avoided by the FPGA internal clocks and PLL (Phase-Locked Loop).

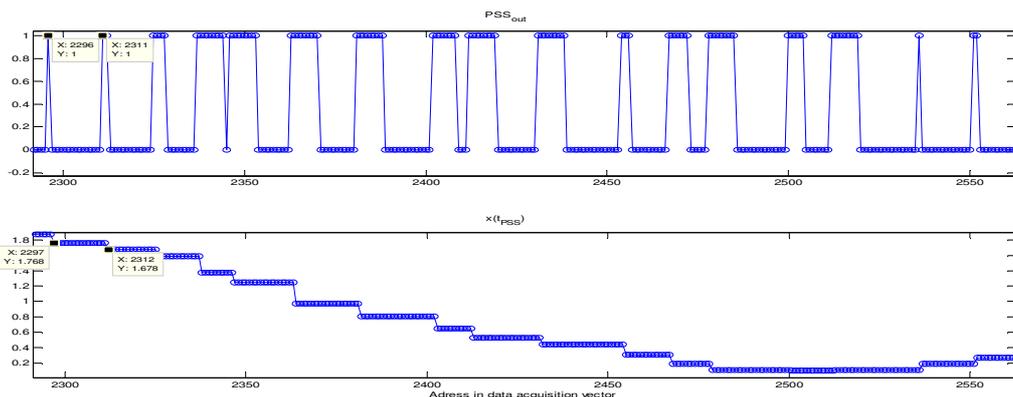


Figure 6. Timing sampling and output ADC

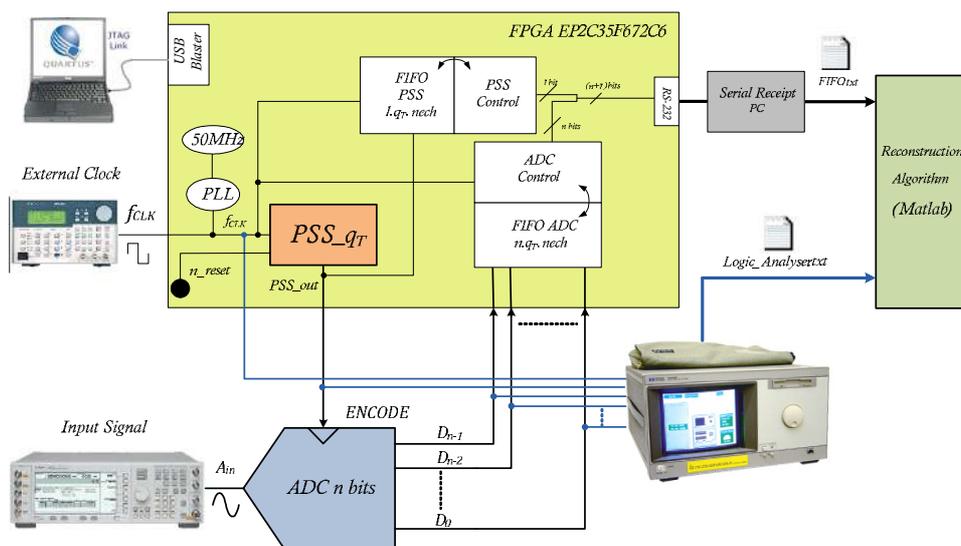


Figure 7. Test platform synoptic

- A sine wave generator delivers analog signal to A_{in} ADC pin. The PSS output is also fed to the $ENCODE$ ADC pin.

- The FIFO based acquisition method is implemented on FPGA. Acquisition control is performed by the main clock.

- ADC digital outputs $D_n \dots D_0$ are taken into a multi-bit FIFO however PSS output is taken into a single bit FIFO.

- Acquisition data is sent through UART (RS232) to DSP board. The signal reconstruction is performed with interpolation algorithm.

- Spectral analysis is performed by Matlab software on data coming from ADC and DSP.

- FPGA configuration is done by Quartus through USB blaster.

We have used digital analyser from Agilent 16700-Series to verify and calibrate the proposed acquisition method.

5.3. ADC Results after reconstruction

For the current results, we achieve our tests with the AD9214 analog-to-digital converter from Analog Devices [7]. Equations (4), (5) and (7) are generally verified by the most commercialized ADCs. The chosen PSS configuration is for q_T equal to 16 because the error compared to $\sigma/T_s = 0.2887$ is only 6.5%. A 100 kHz sine wave is sampled non uniformly at a mean frequency 3.125 MHz. The PSS and acquisition main clock is a 50 MHz square wave. The required FIFO sizes are respectively 16384 bits for the PSS FIFO and 163840 bits for ADC FIFO to reconstruct 1024 uniform samples.

The second step consists on applying PSS output signal on the AD9214 pipeline ADC, PSS and output ADC acquisition, reconstruction and spectrum analysis presented in Figure 8.

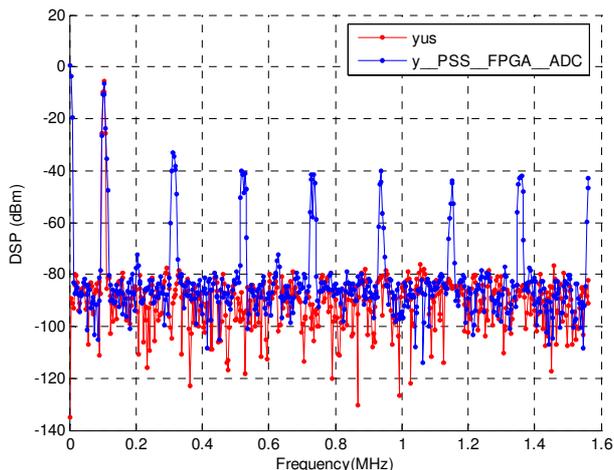


Figure 8. PSS based ADC spectrum analysis after cubic spline reconstruction ($y_{PSS_FPGA_ADC}$) versus uniform sampling spectrum analysis (yus).

We notice odd signal harmonics compared to uniform case. The drawback of the AD9214 to offer the required signal is the fact that the Analog Devices design contains a Timing block as shown in Figure 9. The Timing block is essential in uniform sampling ADC to correct signal

clock. It is designed to correct the modified duty cycle due to any noise, distortion or timing jitter on the clock controlling the ADC and fed to the $ENCODE$ ADC input [7].

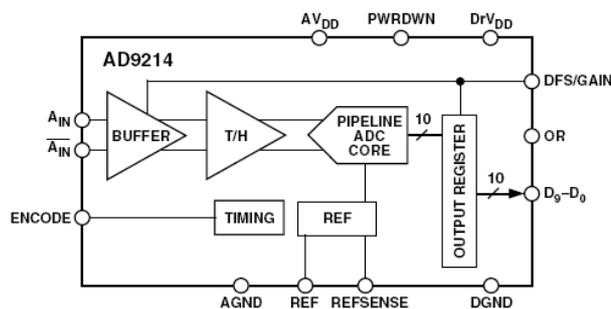


Figure 9. AD9214 Functional Block Diagram.

Applying the PSS output sequence to a S/H Simulink model, then performing spectrum analysis after reconstruction return the spectrum presented in Figure 10. We verify that we recover exactly the same results as in uniform sampling case. The test described above is also done with q_T equal to 32 and results are similar to those in Figures 8 and 10.

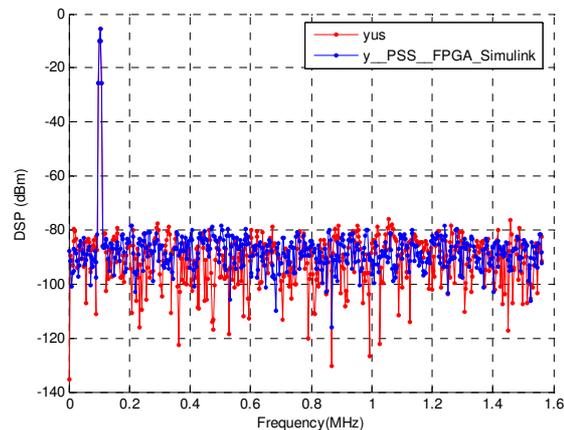


Figure 10. PSS based S/H Simulink Model spectrum analysis after cubic spline reconstruction ($y_{PSS_FPGA_Simulink}$) versus uniform sampling spectrum analysis (yus).

6. CONCLUSION

In this paper, we summarize some interesting theory formulation results on non uniform sampling. In fact, under some conditions, non uniform sampling offers the advantages of anti-aliasing spectrum. This advantage motivates our work to be oriented on the non uniform sampling based baseband stage in multistandard receiver. We are especially interested on the strategy of reducing mean sampling frequency to reduce ADC dynamic power consumption. We propose a pseudorandom signal sampler circuit to control the ADC. From FPGA implementation and synthesis and from implementation on CMOS 65 nm digital technology, we evaluate the attainable maximum frequency and the low power consumption of the PSS circuit.

A test platform is realized and we compare the ADC spectrum analysis and performances in the non uniform sampling case using PSS circuit compared to uniform sampling case at frequency equal to the main clock

frequency of the pseudorandom signal sampler circuit. We obtain some odd harmonics due to timing block required to correct duty cycle. The solution is to replace the pipeline ADC by a full-flash converter. These results for a main clock frequency equal to 50 MHz and results from previous works [1, 2] are optimistic to realize a closer test platform to the multistandard NUS-based homodyne receiver.

7. ACKNOWLEDGMENT

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